Primary Side Quasi-Resonant Controller with MOSFET Integrated

REV. 00

General Description

The LD9162K is an excellent primary-side feedback controller with QR operation, integrated with a 650V MOSFET switch in a SOP-8 package. It minimizes the components counts and is ideal for low cost applications.

It provides functions of ultra-low startup current, green-mode power-saving operation and leading-edge blanking of the current sensing. Also, the LD9162K includes the comprehensive protection function, such as Over Load Protection (OLP), Over Voltage Protection (OVP), and internal Over Temperature Protection (OTP). Furthermore, the programmable brown-in/out protection and bulk cap. OVP protection is built-in.

In most cases, PSR controlled flyback converters would suffer from bad load regulation performance. To deal with this problem, dedicated load regulation compensation is also implemented in LD9162K.

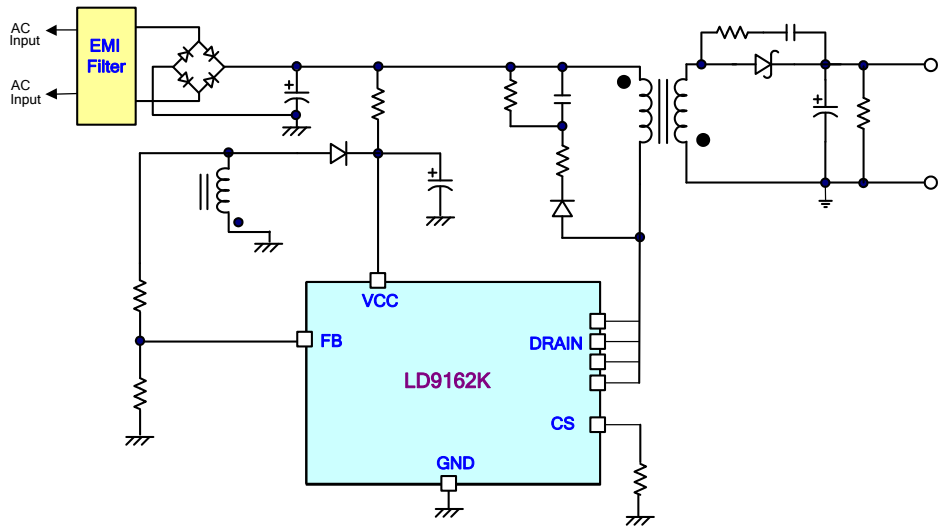
Features

- Primary-Side Feedback Control with Quasi-Resonant Operation
- Built-in 650V MOSFET Switch
- Built-in Load Regulation Compensation
- Constant Current Control
- Ultra-Low Startup Current (<1.9μA)
- 80 kHz Maximum Switching Frequency.
- Green Mode Control to enhance Efficiency
- LEB (Leading-Edge Blanking) On CS Pin
- VCC OVP (Over Voltage Protection)
- Adjustable Brown in/out and Bulk_OVP on FB pin.
- Internal OTP (Over Temperature Protection)
- SDSP (Secondary Diode Short Protection)

Applications

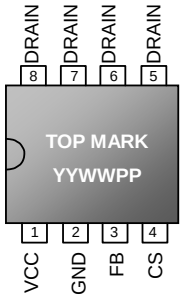
- Mobile Phone Charger
- Low Power AC/DC Adaptor

Typical Application



Pin Configuration

SOP-8 (TOP VIEW)



YY: Year code
WW: Week code
PP: Production code

Ordering Information

Part number	Package	TOP MARK	Shipping
LD9162K GS	SOP-8	LD9162KGS	2500 / tape & reel

The LD9162K is ROHS compliant/ green packaged.

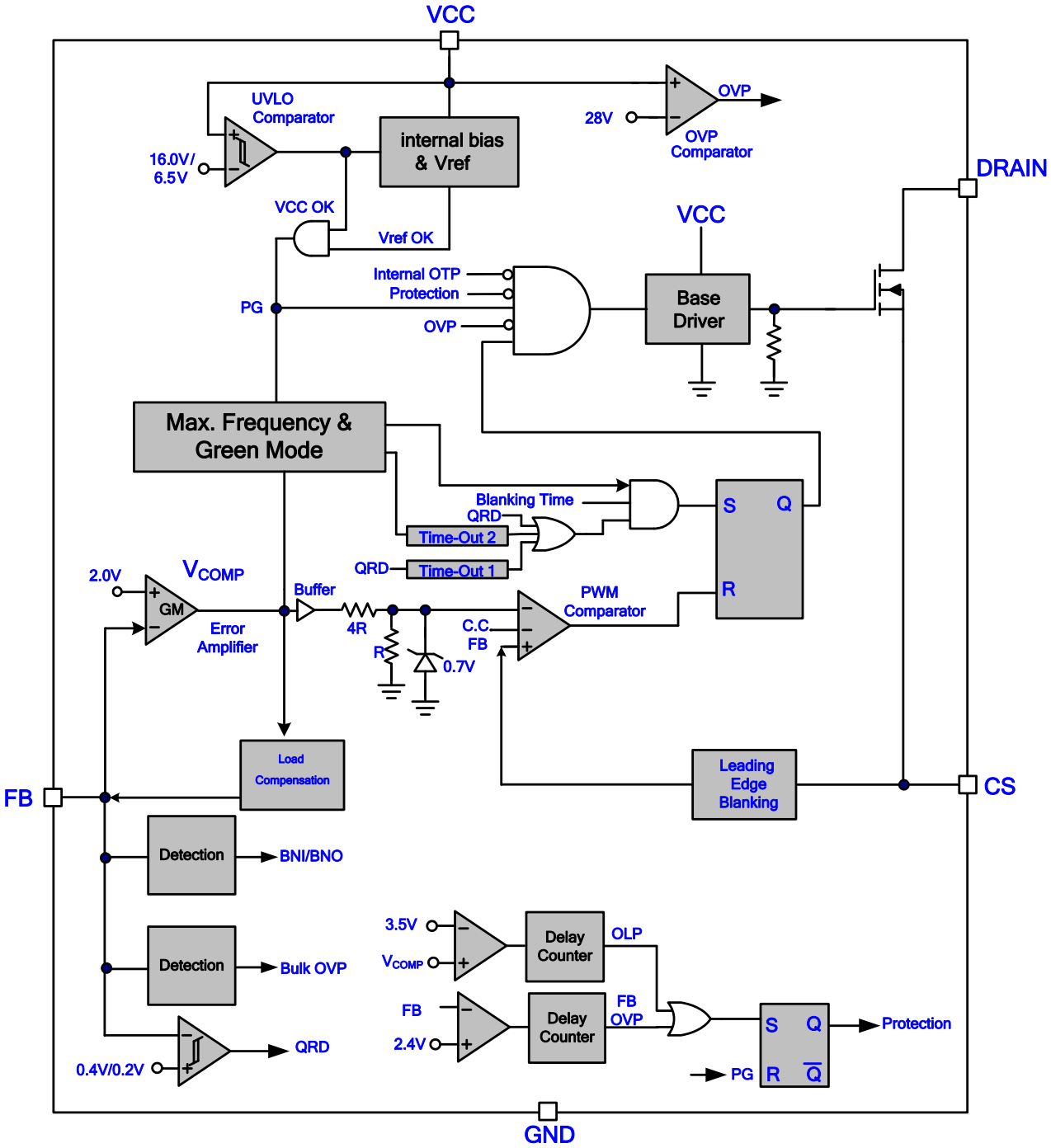
Protection Mode

Part number	VCC_OVP	BULK_OVP	OLP	BNI/BNO	FB_OVP	FB Open/Short	SDSP
LD9162K	Auto-Restart	Auto-Restart	Auto-Restart	Auto-Restart	Auto-Restart	Auto-Restart	Auto-Restart

Pin Descriptions

NAME	PIN (SOP-8)	FUNCTION
VCC	1	Voltage supply pin.
GND	2	Ground
FB	3	Auxiliary voltage sensing and Quasi Resonant detection.
CS	4	Current sense pin, connect it to sense the switch current.
DRAIN	5,6,7,8	The drain of internal power MOSFET

Block Diagram



Absolute Maximum Ratings

Supply Voltage VCC	32V
DRAIN	-0.3V~650V
FB, CS	-0.3V~6.0V
Maximum Junction Temperature	150°C
Storage Temperature Range	-65°C to 150°C
Package Thermal Resistance (SOP-8, θ_{JA})	106°C/W
Junction to Case Thermal Resistance (SOP-8, θ_{JC})	20°C/W
Power Dissipation (SOP-8, at Ambient Temperature = 85°C)	377mW
Lead temperature (Soldering, 10sec)	260°C
ESD Voltage Protection, Human Body Model (DRAIN pin is exclusive)	2.5 KV
ESD Voltage Protection, Machine Model (DRAIN pin is exclusive)	250 V

Note1: The value of θ_{JA} is measured with the device mounted on 1oz one layer FR-4 board, in a still air environment with TA = 25°C. The value in any given application depends on the user's specific board design.

Caution:

Stress exceeding maximum ratings may damage the device. Maximum ratings are stress ratings only. Functional operation above the recommended operating conditions is not implied. Extended exposure to stress above recommended operating conditions may affect device reliability.

Recommended Operating Conditions

Item	Min.	Max.	Unit
Operating Junction Temperature	-40	125	°C
VCC voltage	9	15	V
VCC capacitor	4.7	10	μF
Start-up resistor Value (AC Side, Half Wave)	2	6.2	MΩ

Note:

1. It's essential to connect VCC pin with an SMD ceramic capacitor (0.1μF~0.47μF) to filter out the undesired switching noise for stable operation. This capacitor should be placed close to IC pin as possible.
2. If the peak of the noise coupled in FB pin is higher than 4.0V, an SMD ceramic capacitor with 10pF is recommended to connect the FB and GND pin.
3. The small signal components should be placed to IC pin as possible.

Electrical Characteristics

(T_A = +25°C unless otherwise stated, VCC=12.0V)

PARAMETER	CONDITIONS	SYM.	MIN	TYP	MAX	UNITS
Supply Voltage (Vcc Pin)						
Startup Current	VCC=UVLO-ON-0.1V	I_{CC_ST}		1.0	1.9	μA
Operating Current	V_{COMP}=0V, OUT=open*	I_{CC_OP}		0.65	1.5	mA
UVLO (off)		V_{CC_OFF}	6	6.5	7	V
UVLO (on)		V_{CC_ON}	15	16	17	V
VCC OVP Level		V_{CC_OVP}	26.5	28	29.5	V
QRD (Quasi Resonant Detection, FB Pin)						
Reference Voltage, V_{REF}		V_{REF}	1.98	2.00	2.02	V
FB OVP Level	*	V_{FB_OVP}		2.4		V
Load Compensation Current	V_{CS}=0.55V	I_{LOAD_COMP}	15.5	17	18.5	μA
Current Sensing (CS Pin)						
Maximum Input Voltage, $V_{CS(OFF)}$		V_{CS_MAX}	0.65	0.7	0.75	V
Minimum V_{CS-OFF}	At Low Line	$V_{CS\_MIN\_L}$	0.15	0.165	0.18	V
	At High Line*	$V_{CS\_MIN\_H}$		0.125		V
Leading Edge Blanking Time		T_{LEB}	300	450	600	ns
QRD (Quasi Resonant Detection, FB Pin)						
QRD Trip Level	*	V_{QRD}		400		mV
	Hysteresis*	V_{QRD_HYS}		200		mV
Brown In Trip Level	*	I_{BNI}	85	95	105	μA
Brown Out Hysteresis	*	I_{BNO_HYS}		10		μA
Brown Out De-bounce Time	*	T_{DB_BNO}		70		ms
Bulk cap OVP level	*	I_{BULK_OVP}	350	380	410	μA
Bulk cap OVP delay	*	T_{BULK_OVP}		450		ms
Oscillator for Switching Frequency						
Maximum Frequency		F_{SW_MAX}	72	80	88	kHz
Minimum Frequency		F_{SW_MIN}	1.35	1.5	1.65	kHz
Maximum On Time		T_{ON_MAX}	22	25	30	μs
SDSP (Secondary Diode Short Protection)						
SDSP CS Pin Level	Secondary diode short*	V_{CS_SDSP}		1.2		V

PARAMETER	CONDITIONS	SYM.	MIN	TYP	MAX	UNITS
SDSP (Secondary Diode Short Protection)						
De-bounce Cycle	Counts in 20ms*	T_{D_SDSP}		6		Cycle
OLP (Over Load Protection)						
OLP Delay time	*	T_{D_OLP}		50		ms
On Chip OTP (Over Temperature)						
OTP Level	*	T_{INOTP}		140		°C
OTP Hysteresis	*	T_{INOTP_HYS}		22		°C
MOSFET Drain (DRAIN Pin)						
Breakdown Voltage		V_{DS}	650			V
On Resistance		R_{DS_ON}		4.5		Ω

*: Guaranteed by design.

Typical Performance Characteristics

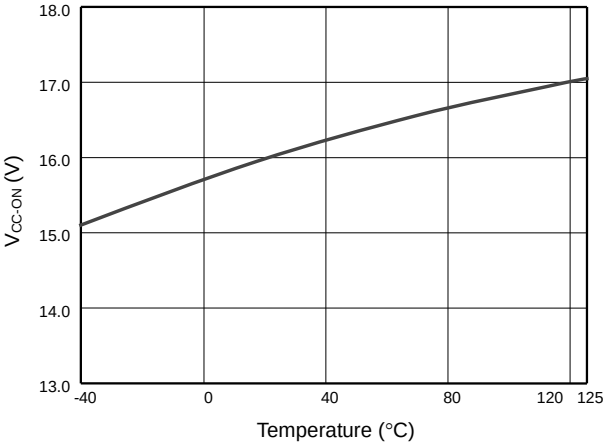


Fig. 1 UVLO (on) vs. Temperature

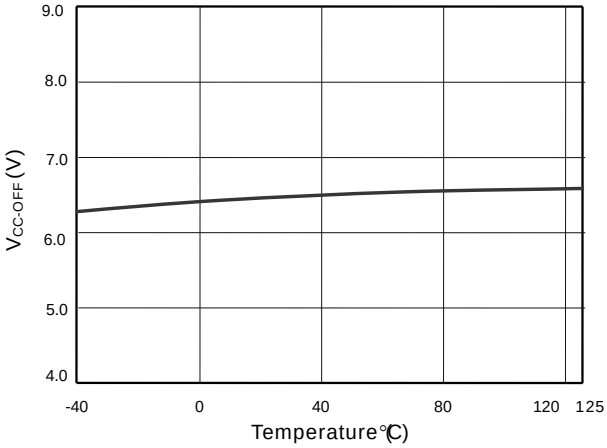


Fig. 2 UVLO (off) vs. Temperature

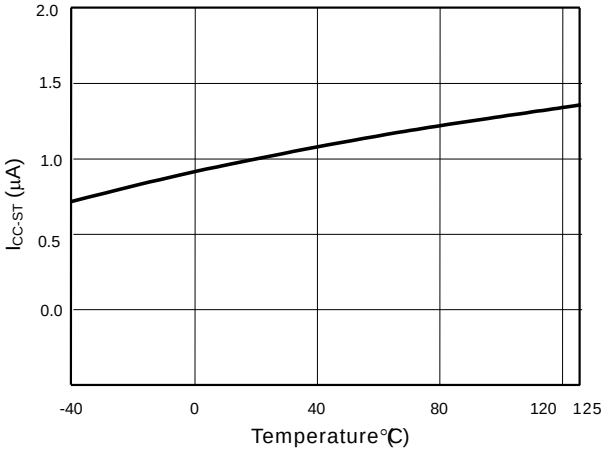


Fig. 3 Startup Current vs. Temperature

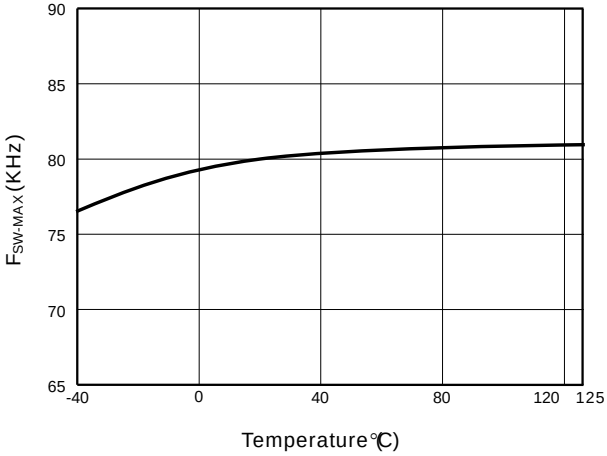


Fig. 4 Max Frequency vs. Temperature

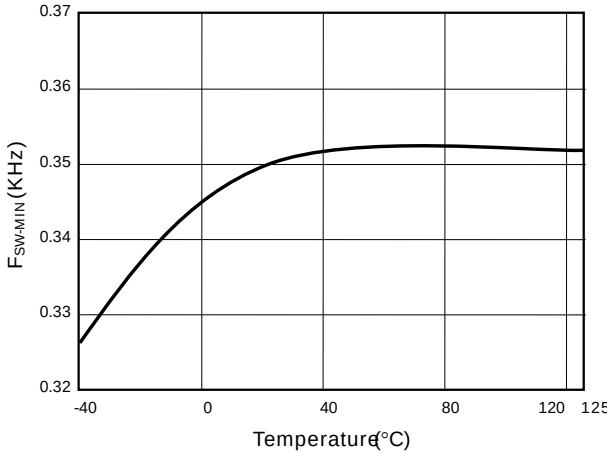


Fig. 5 Min Frequency vs. Temperature

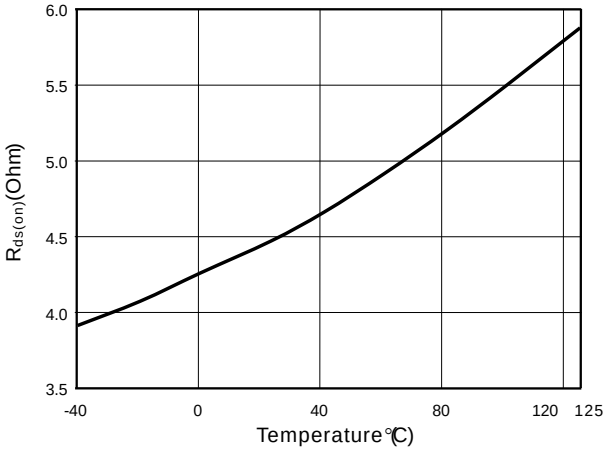


Fig. 6 $R_{ds(on)}$ vs. Temperature

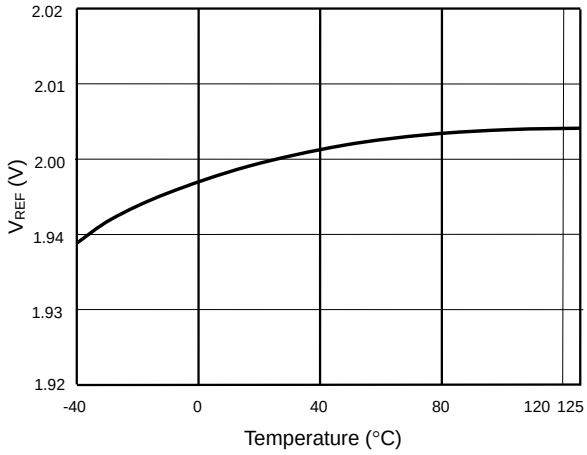


Fig. 7 Reference Voltage vs. Temperature

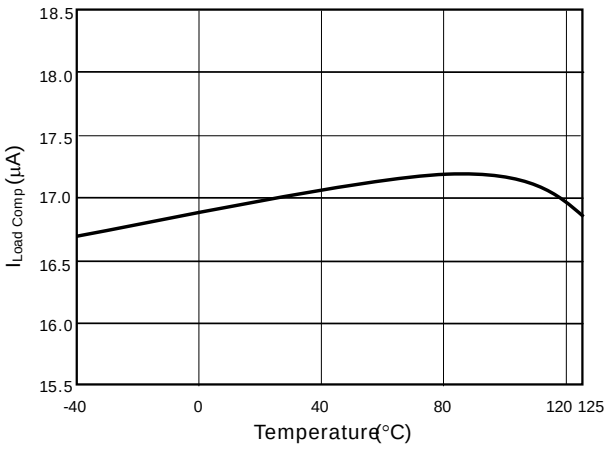


Fig. 8 Load Compensation vs. Temperature

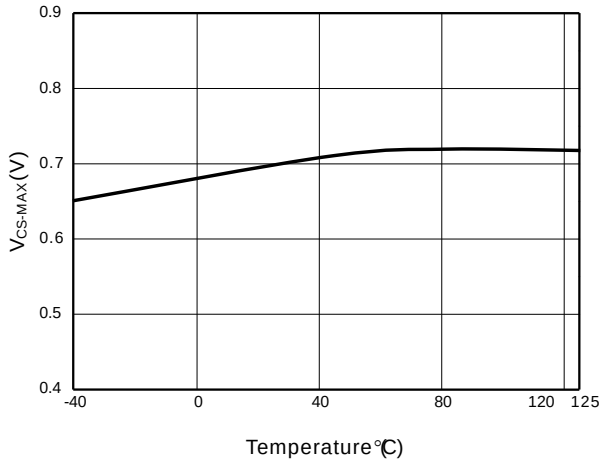


Fig. 9 V_{CSMAX} vs. Temperature

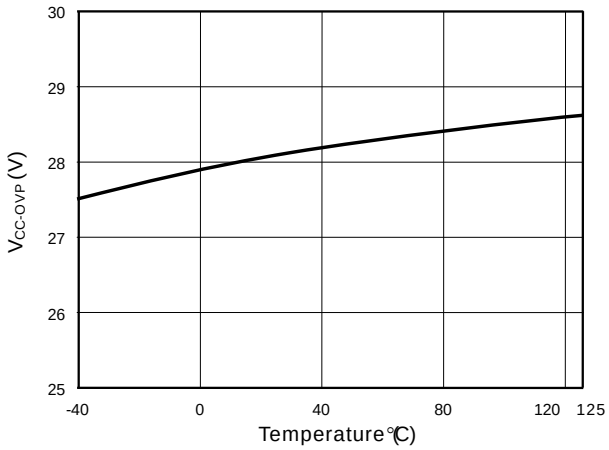


Fig. 10 VCC OVP vs. Temperature

Application Information

Operation Overview

The LD9162K is an excellent primary-side feedback controller with integrated MOS switch to provide a minimum components solution. The LD9162K removes the need for secondary feedback circuits while achieving excellent line and load regulation. It meets the green-power requirement and is intended for the use in those modern switching power suppliers and linear adaptors that demand higher power efficiency and power-saving. It is built-in with several functions to reduce the external components counts and the size. The major features are described as below.

Under Voltage Lockout (UVLO)

An UVLO comparator is implemented to detect the voltage on the VCC pin. The supply voltage should be large enough to turn on the controllers and further drive the power MOS. As shown in Fig. 11, a hysteresis window is built in to prevent the shutdown from unwanted voltage dip during the start-up.

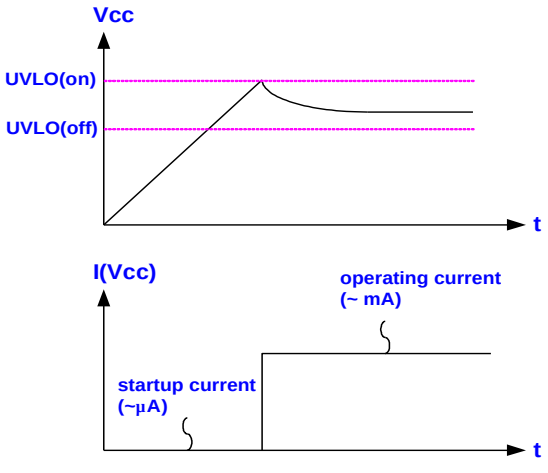


Fig. 11

Startup Current and Startup Circuit

The typical startup circuit to generate VCC of the LD9162K is shown in Fig. 12. At startup transient, the VCC is below the UVLO_ON threshold, so LD9162K will not work in this condition. Therefore, the current through R1 will be used to charge the capacitor C1. Until the VCC is fully charged to enable the LD9162K to start switching, the auxiliary winding will provide the supply power instead. If PWM controller requires less current to start up, it will allow less power consumption on R1. By using CMOS process and some unique circuit design, the LD9162K requires only 1.9μA max to start up. Higher resistance of R1 will spend much more time to start up. The user is recommended to select proper value of R1 and C1 to optimize the power consumption and startup time.

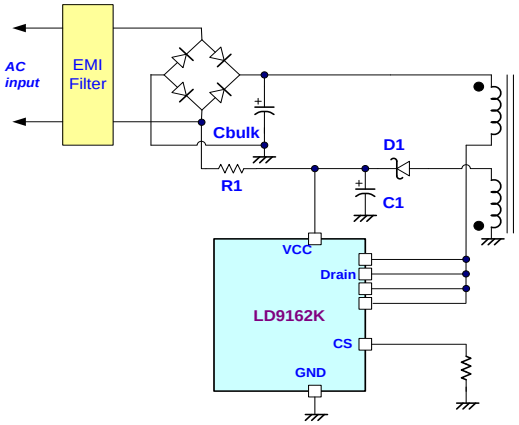


Fig. 12

Principle of CV Operation

In the DCM flyback converter, it senses the output voltage through auxiliary winding. LD9162K samples the auxiliary winding on the primary-side to regulate the output voltage, as shown in the Fig. 13. The voltage induced in the auxiliary winding is a reflection of the secondary winding voltage while the MOS is in off state. Via a resistor divider connected between the auxiliary winding and FB pin, the

auxiliary voltage is sampled after the sample delay time and will be held until the next sampling. The sampled voltage is compared with internal reference V_{REF} and the error will be amplified. The error amplifier output COMP reflects the load condition and controls the duty cycle to regulate the output voltage, thus constant output voltage can be achieved. The output voltage is given as:

$$V_{OUT}=2.0V\times\left(1+\frac{R_a}{R_b}\right)\left(\frac{N_s}{N_a}\right)-V_F$$

Where V_F indicates the drop voltage of the output Diode, Ra and Rb are top and bottom feedback resistor value, Ns and Na are the turns of transformer secondary and auxiliary.

In case that the output voltage is sensed through the auxiliary winding; the leakage inductance will induce ringing to affect output regulation. To optimize the drain voltage, a proper clamp circuit will minimize the high frequency ringing and achieve the best regulation. Fig. 14 shows the desired drain voltage waveform in compare to those with large undershoot due to leakage inductance induced ring (Fig. 15). This will make the sample error and cause poor performance for output voltage regulation. A proper selection for resistor R_S, in series with the clamp diode, may reduce any large undershoot, as shown in Fig. 13.

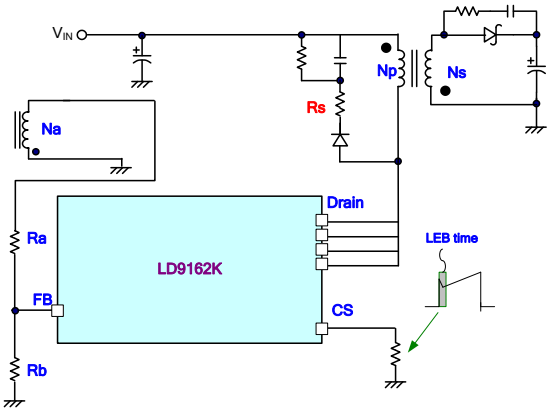


Fig. 13

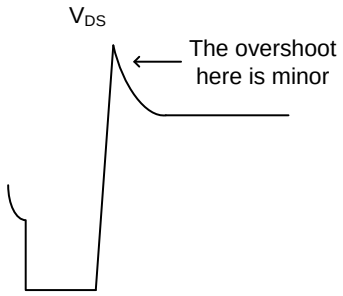


Fig. 14

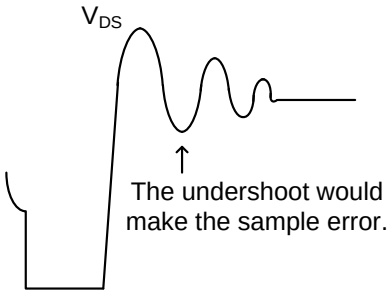


Fig. 15

Load Regulation Compensation

With the purpose of keeping the voltage of the cable end constant, LD9162K is implemented with the load regulation compensation to counteract the cable voltage drop. The compensated voltage is created by sinking a certain current through the FB pin during the sampling period. The internal sinking current source is proportional to the value of V_{CS}, as shown in Fig. 16. Therefore, the voltage drop caused by the cable loss can be compensated as the load becomes heavy. It can also be programmed by adjusting the resistance of the voltage divider to compensate for different types or length of cable lines. The equation of the internal sink current is shown as:

$$I_{LOAD\_COMP}\cong Vcs\times 25.83\ (\mu A)$$

The percentage of maximum compensation is shown as:

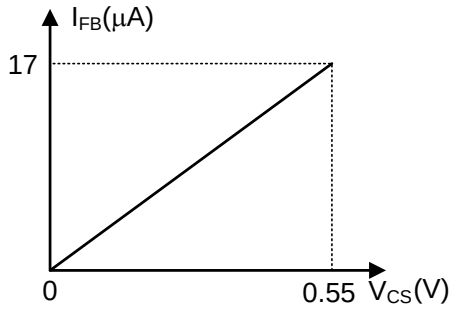


Fig. 16

Quasi-Resonant Mode Detection

LD9162K employs quasi-resonant (QR) switching scheme to switch at the valley of the drain voltage.

This feature is able to reduce the switching loss and dv/dt in the operating range of the power supply substantially. The QR detection comparator detects the FB pin after the switch is turned off, and triggers QRD signal if the voltage drops to 0.2V. The QRD signal remains low if V_{FB} stays above 0.4V. Under light load condition, the resonant signal damps gradually. After the QRD signal disappears for a certain time interval, defined as time-out 1, the controller is forced to turn on the switch as soon as the limited period ends.

Multi-Mode Operation

The controller changes its operating frequency according to the load condition and line voltage.

At heavy load condition, the operating frequency may change according to the line voltage. If the AC input is in low line, the controller usually turns on at the first valley because of the large duty cycle and long period time. If in high line, the switching frequency increases till it reaches the limit and skips the first valley to turn on at the 2nd, 3rd….valley. The switching frequency varies generally when the system is operated in QR mode.

At medium load conditions, the frequency clamp is reduced to 25 kHz maximum. However, the characteristic in valley switching behaves as well. The LD9162K turns on the switch at the 3rd, 4th… valley. That is, when the load decreases, the system automatically skips some valleys and the switching frequency is thereby limited. Therefore, the smooth frequency fold-back and high power efficiency are achieved.

At no load or ultra-light load conditions, the system operates in minimum frequency for lower power saving. LD9162K modulates the frequency according to the load.

Current Sensing and Leading-Edge Blanking

The typical current mode of PWM controller feedbacks both current signal and voltage signal to close the control loop and achieve regulation. As shown in Fig. 13, the LD9162K detects the primary MOS current from the CS pin, which is not only for the peak current mode control but also for the pulse-by-pulse current limit. The maximum voltage threshold for the current sensing pin is set at 0.7V. From above, the MOS peak current can be obtained from below.

$$I_{PEAK(MAX)} = \frac{0.7V}{R_{CS}}$$

A leading-edge blanking (LEB) time is included in the input of CS pin to prevent the false-trigger from the current spike.

High/Low Line Detection

LD9162K has setting the high/low line detect voltage through (Ra), assume that V_{HL_H} is the boundary voltage between high/low line detect level. The equation of Ra is shown as:

$$R_a = \frac{V_{HL\_H} \times \sqrt{2} \times \frac{N_a}{N_P}}{205\mu A}$$

The low line current as 197μA, according to the Ra value the C.C. compensation will adjust at different lines voltage.

Principle of C.C. Operation

The primary side control scheme is applied to eliminate secondary feedback circuit or opto-coupler, which will reduce the system cost. The switching waveforms are shown in Fig. 17. The output current "Io" can be expressed as:

$$Io = \frac{1}{2} \frac{i_{S,PK} \times T_{DIS}}{T_S}$$
$$= \frac{1}{2} \frac{N_P}{N_S} \times i_{P,PK} \times \frac{T_{DIS}}{T_S}$$
$$= \frac{1}{2} \frac{N_P}{N_S} \times \frac{V_{CS}}{R_{CS}} \times \frac{T_{DIS}}{T_S}$$

The primary peak current ($i_{P,PK}$), inductor current discharge time (T_{DIS}) and switching period (T_S) can be detected by the IC. The ratio of $V_{CS}*T_{DIS}/T_S$ will be modulated as a constant ($V_{CS}*T_{DIS}/T_S$ =1/3), so that I_O can be obtained as

$$Io = \frac{1}{2} \frac{N_P}{N_S} \times \frac{V_{CS}}{R_{CS}} \times \frac{T_{DIS}}{T_S}$$
$$= \frac{1}{2} \frac{N_P}{N_S} \times \frac{1}{R_{CS}} \times \frac{1}{3}$$

However this is an approximate equation. The user may fine-tune it according to the experiment result.

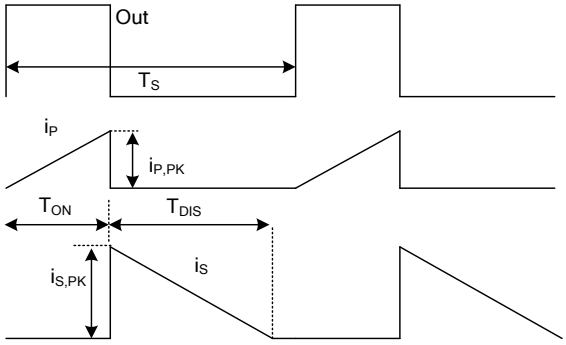


Fig. 17

Over Load Protection (OLP) - Auto Recovery

To protect the circuit from damage in over-load condition or open-loop fault, LD9162K is implemented with the smart OLP function. It also features auto recovery mechanism, referring to Fig. 18. In detail, if the protection condition is removed, the VCC level will get back to normal and the output will automatically return to the normal operation.

In the case of fault condition, the voltage loop is forced toward saturation and then pulls the voltage high on the COMP signal. When it ramps up to the OLP threshold voltage and stays longer than the delay time, the protection is activated when the output gate signals are forced to stop.

With the protection mechanism, the average input power is minimized to remain the component temperature and stress within the safe operating area (SOA).

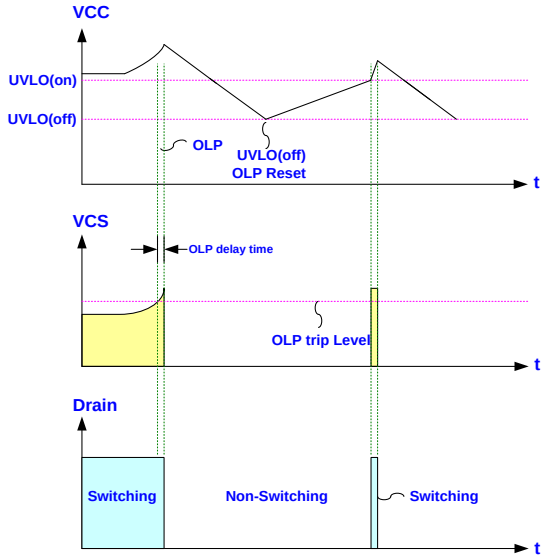


Fig. 18

OVP (Over Voltage Protection) on VCC – Auto Recovery

LD9162K is implemented with OVP function over VCC. As the VCC voltage rises over the OVP threshold voltage, the output drive circuit will be shutdown simultaneously to stop the switching of the power MOS until the next UVLO (on) arrives. The VCC OVP function of LD9162K is an auto-recovery type protection. The Fig. 19 shows its operation. On the other hand, if the OVP condition is removed, the VCC level will get back to normal level and the output will automatically return to the normal operation.

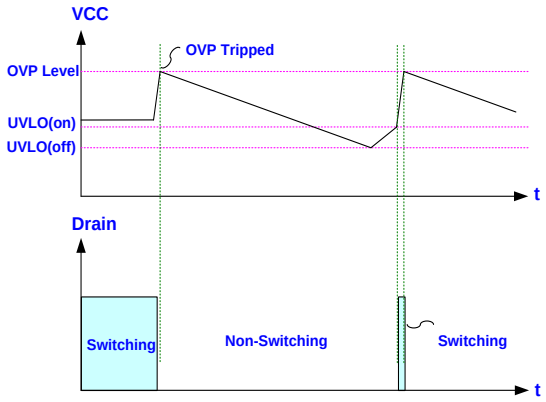


Fig. 19

Brown-In/ Brown-Out Protection (BNI/BNO) and Bulk Cap OVP– Auto Recovery

The LD9162K integrates the brown in, brownout protection and valley detection into FB pin. The auxiliary voltage reflects a proportional bulk voltage during the on time. Fix the internal current at the BNI, BNO and BULK_OVP, the BNI level could be set by modulating the FB divided resistors and auxiliary voltage, as shown in Fig. 13. For preventing the abnormal condition of line voltage to causing damage, BNO function is implemented, while turns off the gate signal after de-bounce time 70ms as BNO occurring, as shown in Fig. 20. The BULK_OVP is implemented as shown in Fig. 21. The gate signal will be turned off after de-bounce time 450ms, while I_{BULK_OVP} is tripped. If V_{BULK} over $V_{DC\_BULK\_OVP}$ before start up then de-bounce time is 5ms. The relationship of input voltage and BNI/BNO and BULK_OVP is as follows.

$$V_{DC\_BNI} = \frac{N_P}{N_a} \cdot I_{BNI} \cdot R_a$$

$$V_{DC\_BNO} = \frac{N_P}{N_a} \cdot I_{BNO} \cdot R_a$$

$$V_{DC\_BULK\_OVP} = \frac{N_P}{N_a} \cdot I_{BULK\_OVP} \cdot R_a$$

Where

V_{DC_BNI} is predicted BNI DC value of input voltage.

V_{DC_BNO} is predicted BNO DC value of input voltage.

$V_{DC\_BULK\_OVP}$ is predicted BULK_OVP DC value of input voltage.

I_{BNI} is BNI trip current, I_{BNO} is BNO trip current.

I_{BULK_OVP} is BULK OVP trip current.

Np is turns ration of primary-side winding.

Na is turns ration of auxiliary winding.

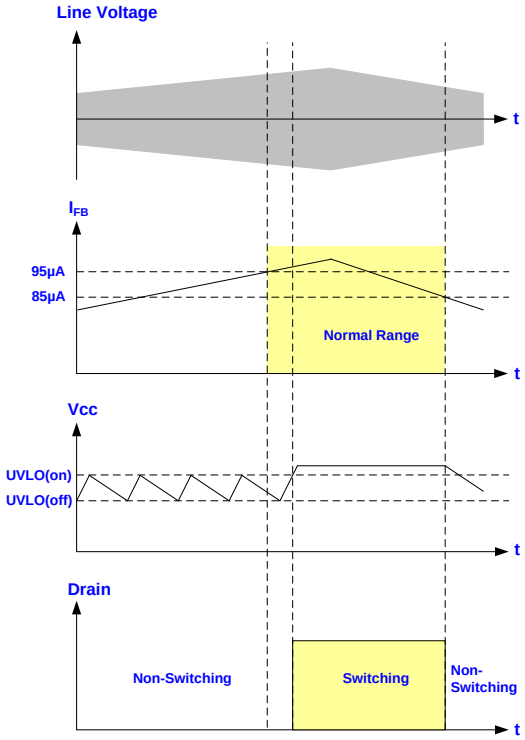


Fig. 20

Over Voltage Protection on FB Pin (FB OVP) – Auto Recovery

An output overvoltage protection is implemented in the LD9162K. The auxiliary winding voltage can be reflected from secondary winding, in which the FB pin voltage is proportional to output voltage during the gate off time. OVP is worked by sensing the auxiliary voltage via the divided resistors R_b, refereeing to Fig. 22. If V_{FB} overs the FB OVP trip level, the internal counter starts counting 6 cycles, and then LD9162K goes to auto-recovery protection mode till the FB OVP status is defused.

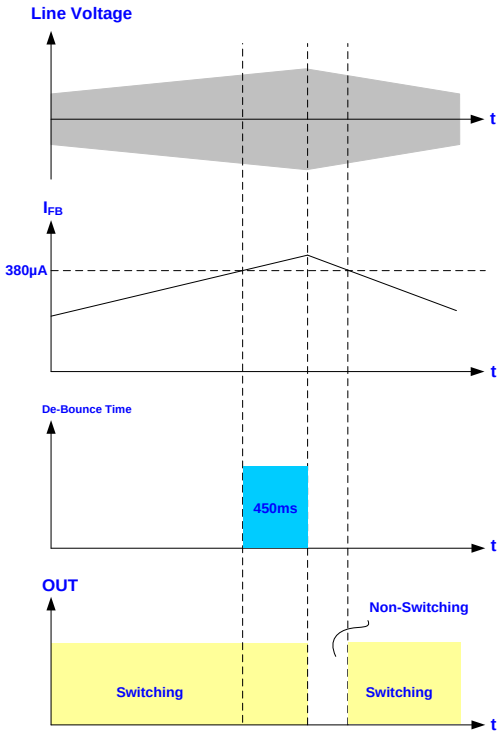


Fig. 21

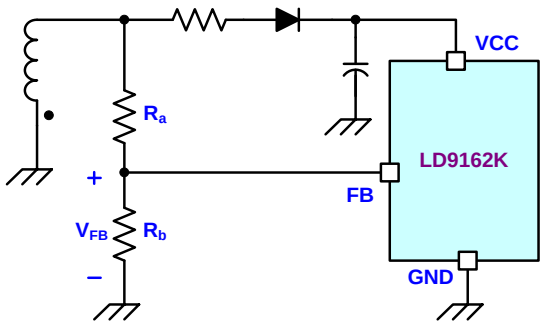


Fig. 22

Secondary Diode Short Protection (SDSP) – Auto Recovery

The logic of SDSP is described briefly as follows. If VCS is higher than 1.2V, the count is up to 6 times in 20ms. Its gate will be turned-off, shown as Fig. 23.

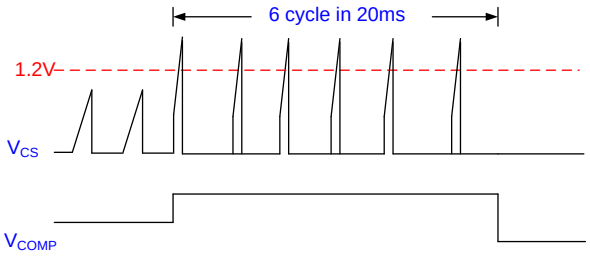
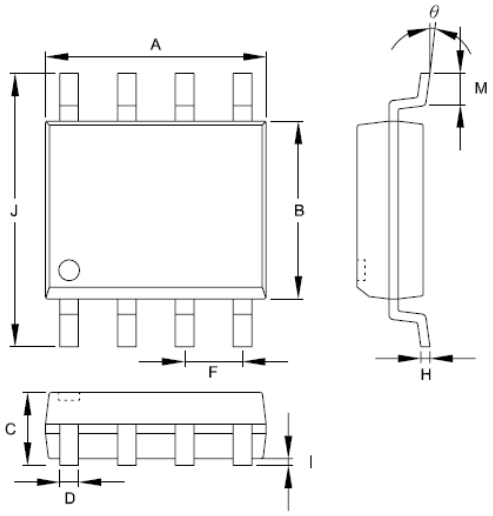


Fig. 23

Package Information

SOP-8



Symbol	Dimensions in Millimeters		Dimensions in Inch	
	MIN	MAX	MIN	MAX
A	4.801	5.004	0.189	0.197
B	3.810	3.988	0.150	0.157
C	1.346	1.753	0.053	0.069
D	0.330	0.508	0.013	0.020
F	1.194	1.346	0.047	0.053
H	0.178	0.254	0.007	0.010
I	0.102	0.254	0.004	0.010
J	5.791	6.198	0.228	0.244
M	0.406	1.270	0.016	0.050
θ	0°	8°	0°	8°

Revision History

REV.	Date	Change Notice
00	03/10/2021	Original Specification