Multi-Mode PWM Controller of Flyback with MOSFET Integrated

REV. 00

General Description

The LD9535K is built in a multi-mode PWM controller and integrated a 650V MOSFET. The multi-mode PWM controller which consists of Quasi-Resonant (QR) PWM control for light load condition and Continue Conduction Mode (CCM) for heavy load condition. Moreover, the QR controller not only gains the system performance, but also brings the worse EMI capability, while the frequency swapping function of LD9535K can reduce the EMI emission of SMPS and helps the power circuit designers to simply deal with EMI filter and saves several component and developing time.

The LD9535K is implemented in DIP-8 package, and includes the comprehensive protection function, such as Over Load Protection (OLP), Over Voltage Protection (OVP), Output Short Circuit Protection (OSCP) and internal Over Temperature Protection (OTP).

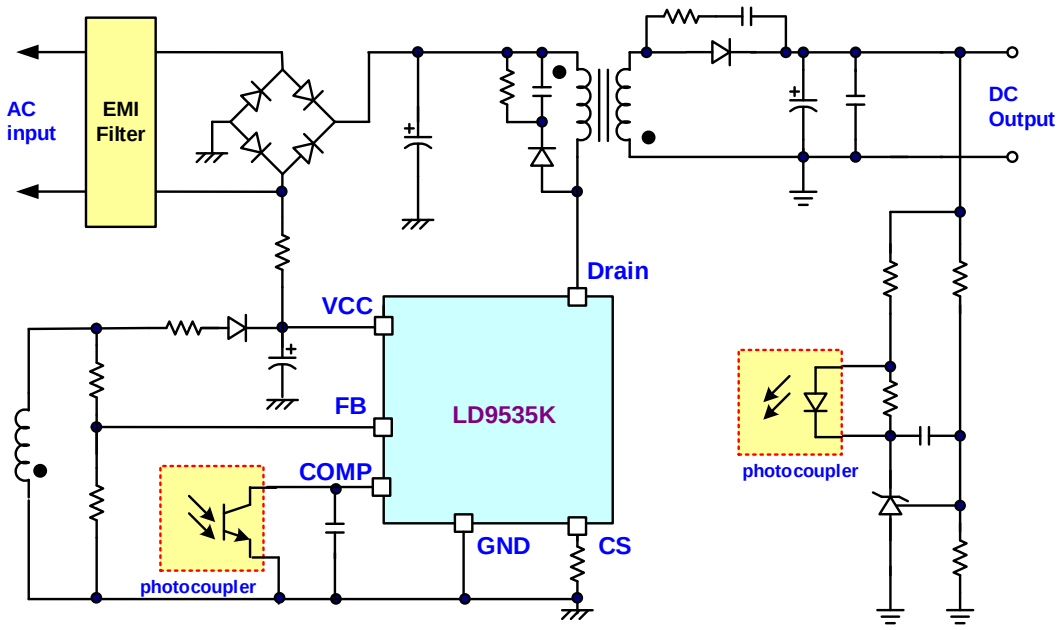
Features

- Secondary-side feedback control with quasi-resonant + CCM operation
- Built-in 650V MOSFET Switch
- Low Startup Current (<1μA)
- Ultra-low operating current at light load
- Current Mode Control with Cycle-by-Cycle Current Limit
- Green Mode Control
- UVLO (Under Voltage Lockout)
- LEB (Leading-Edge Blanking) on CS Pin
- VCC OVP (Over Voltage Protection)
- Adj. OVP / UVP on FB pin
- Adj. BNI/BNO, Bulk cap. OVP on FB pin
- OLP (Over Load Protection)
- Internal OTP (Over Temperature Protection)

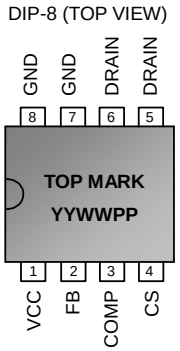
Applications

- Switching AC/DC Adaptor

Typical Application



Pin Configuration



YY: Year code
WW: Week code
PP: Production code

Ordering Information

Part number	Package		TOP MARK	Shipping
LD9535KGN	DIP-8	(Green Package)	LD9535KGN	3600 /tube /carton

The LD9535K is RoHs compliant/ green packaged.

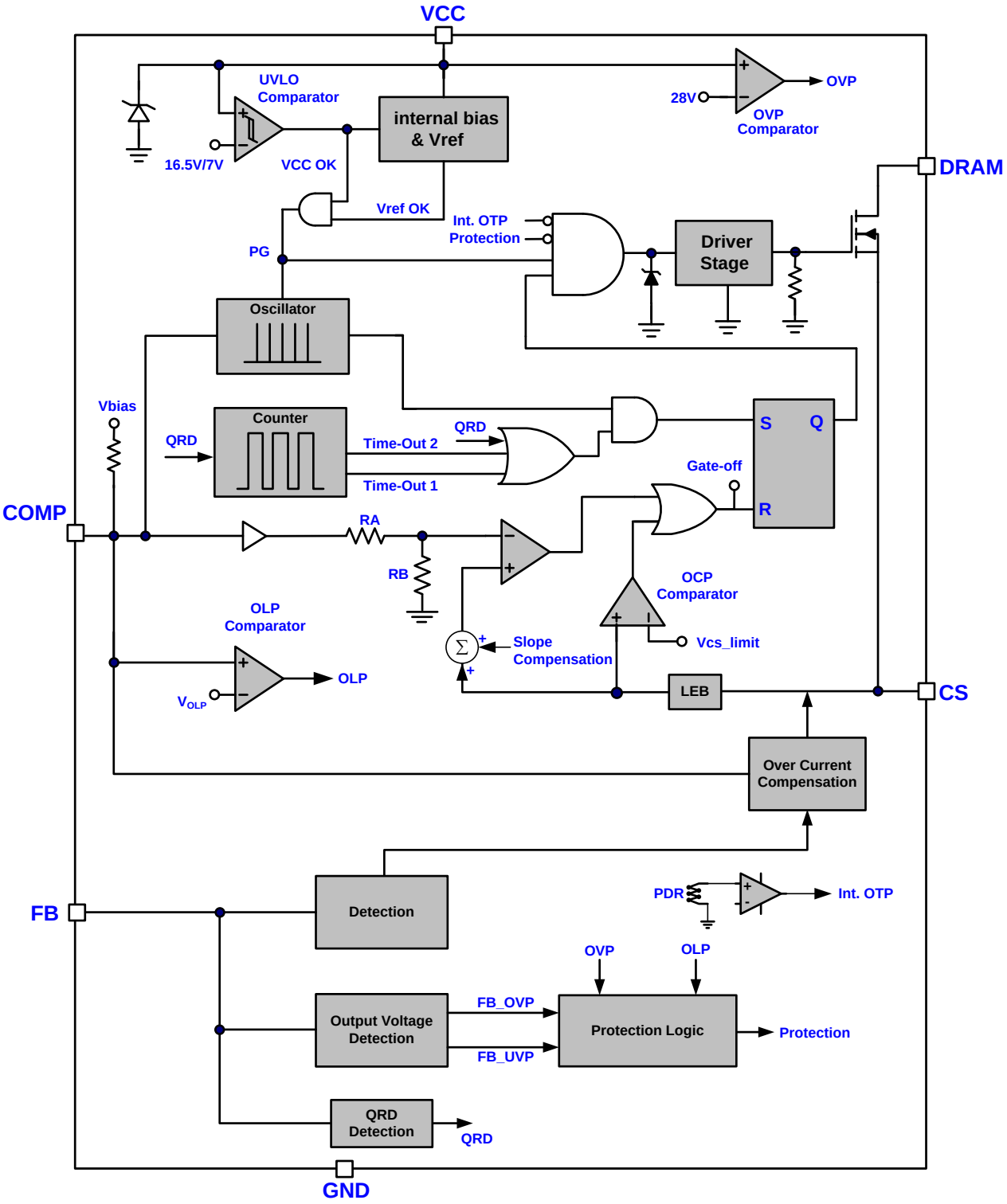
Protection Mode

Product Name	Switching Freq.	Bulk cap OVP	VCC_OVP	FB_OVP	OSCP	OLP	Int. OTP
LD9535K	65kHz	Auto recovery	Auto recovery	Auto recovery	Auto recovery	Auto recovery	Auto recovery

Pin Descriptions

NAME	Pin (DIP-8)	FUNCTION
GND	8,7	Ground
DRAIN	5,6	The drain of internal power MOSFET
CS	4	Current sense pin, connect to sense the MOSFET current
COMP	3	Output of the error amplifier for voltage compensation
FB	2	Auxiliary voltage sense and Quasi Resonant detection
VCC	1	Supply voltage pin

Block Diagram



Absolute Maximum Ratings

Supply Voltage VCC	-0.3V ~ 30V
COMP	-0.3V ~ 12V
FB, CS	-0.3V ~ 7V
DRAIN	-0.3V ~ 650V
Drain Peak Current	4A
Maximum Junction Temperature	150°C
Storage Temperature Range	-65°C ~ 150°C
Package Thermal Resistance (DIP-8, θ_{JA})	80°C/W
Package Thermal Resistance (DIP-8, θ_{JC})	30°C/W
Total Power Dissipation (DIP-8, at Ambient Temperature = 85°C)	500mW
Lead temperature (Soldering, 10sec)	260°C
ESD Voltage Protection, Human Body Model (Except Drain Pin)	2.5 KV
ESD Voltage Protection, Human Body Model (Drain Pin)	1 KV
ESD Voltage Protection, Machine Model (Except Drain Pin)	250 V
ESD Voltage Protection, Machine Model (Drain Pin)	200 V

Caution:

Stress exceeding maximum ratings may damage the device. Maximum ratings are stress ratings only. Functional operation above the recommended operating conditions is not implied. Extended exposure to stress above recommended operating conditions may affect device reliability.

Note 1: The value of θ_{JA} is measured with the device mounted on 1oz one layer FR-4 board, in a still air environment with TA = 25°C. The value in any given application depends on the user's specific board design.

Note2: When CS pin negative spike voltage < -2V, the time must be < 200ns at every duty cycle. (The state of note 2 simply happens when user's system is designed according to the application information.)

Recommended Operating Conditions

Item	Min.	Max.	Unit
Operating Junction Temperature	-40	125	°C
Supply VCC Voltage	8.0	26.5	V
VCC Capacitor	3.3	10	μF
Start-up resistor Value (AC Side, Half Wave)	400K	2M	Ω
Comp Pin Capacitor (X7R type)	330	4700	pF
CS Pin Capacitor Value		30	pF

Note:

1. It's essential to connect VCC pin with a SMD ceramic capacitor (0.1μF ~ 0.47μF) to filter out the undesired switching noise for stable operation. This capacitor should be placed close to IC pin as possible.
2. It's also essential to connect a capacitor to COMP to filter out the undesired switching noise for stable operation.
3. The small signal components should be placed close to IC pin as possible.

Electrical Characteristics

(T_A = +25ºC unless otherwise stated, VCC=15.0V)

PARAMETER	CONDITIONS	SYMBOL	MIN	TYP	MAX	UNITS
Supply Voltage (VCC Pin)						
Startup Current		I_{CC_ST}			1	μA
Operating Current	V_{COMP}=0V	I_{CC_OP1}		0.295		mA
	V_{COMP}=1.7V,I_{FB}=200μA	I_{CC_OP2}		1.95		mA
	Auto current protection	I_{CC_OPA1}		0.6		mA
UVLO(OFF)		V_{CC_OFF}	6	7	8	V
UVLO(ON)		V_{CC_ON}	15.5	16.5	17.5	V
VCC OVP Level		V_{CC_OVP}	27	28	29	V
VCC OVP de-bounce time		T_{VCC_OVP}		8		Cycle
Voltage Feedback (COMP Pin)						
Short Circuit Current	V_{COMP}=0V	I_{COMP}	0.08	0.116	0.15	mA
Open Loop Voltage	(1)	V_{COMP_OPEN}		3.15		V
Current Sensing (CS Pin)						
Maximum Input Voltage	I_{FB}=0μA	V_{CS_LIMIT}	0.45	0.5	0.55	V
Leading Edge Blanking Time	(1)	T_{LEB}		450		ns
Internal Slope Compensation	ton>3μs to D_{MAX}. (Linearly increase), (1)	V_{SLP_L}		220		mV
QRD (Quasi Resonant Detection, FB Pin)						
FB OVP Trip voltage Level		V_{FB_OVP}	3.3	3.5	3.7	V
FB OVP De-bounce Time		T_{FB_OVP}		8		Cycle
FB UVP Trip voltage Level	(1)	V_{FB_UVP}		0.8		V
QRD Trip Level	(1)	I_{QRD}		20		μA
Oscillator for Switching Frequency						
CCM Frequency		F_{CCM}	60	65	70	kHz
Frequency Swapping	(1)	F_{SW_MOD}		±8		%
Green Mode Frequency		F_{SW_GREEN}	21	24	27	kHz
Temp. Stability	(1)	F_{SW_TS}		3	5	%
Voltage Stability	VCC =9V~24V (1)	F_{SW_VS}			1	%
Maximum Duty	(1)	D_{MAX}		81		%
Soft Start						
Soft Start Time	V_{CS_OFF} from 0.2V to 0.5V (1)	T_{SS}		7		ms

PARAMETER	CONDITIONS	SYMBOL	MIN	TYP	MAX	UNITS
BNO Protection (FB Pin)						
Brown In Trip Level		I_{BNI}	85	95	105	μA
BNO Hysteresis		I_{BNO_HYS}		10		μA
Brown Out De-bounce Time	V_{COMP}=1.7V	T_{DB_BNO}		75		ms
Bulk Cap OVP		I_{BULK_OVP}		430		μA
Bulk Cap OVP delay	V_{COMP}=1.7V	T_{FB_BOVP}		520		ms
Open Loop Protection						
OLP Trip Level		V_{OLP}	2.65	2.8	2.95	V
OLP delay time	After soft-start	T_{D_OLP}		88		ms
On Chip OTP (Over Temperature Protection)						
OTP Level	(1,2)	T_{INOTP}		140		°C
OTP Hysteresis	(1,2)	T_{INOTP_HYS}		12		°C

Electrical Characteristics for MOSFET

PARAMETER	CONDITIONS	SYMBOL	MIN	TYP	MAX	UNITS
LD9535K MOSFET Drain (DRAIN Pin)						
Breakdown Voltage	VCC=0V , COMP=0V, I_D=250μA , T_j=25°C	BV_{DS}	650			V
	VCC=0V , COMP=0V, I_D=250μA , T_j=125°C (1)		700			V
On Resistance	(1)	R_{DS_ON}		1.4	1.82	Ω

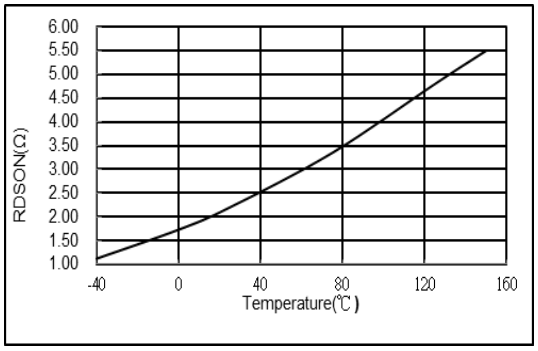


Fig. 1 LD9535K R_{DS_ON} vs. Temperature

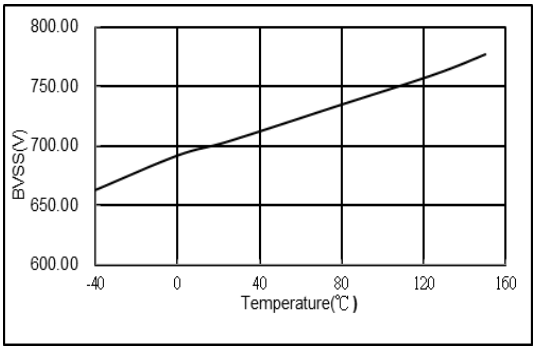


Fig. 2 LD9535K Breakdown Voltage vs. Temperature

Notes:

1. Guaranteed by design.
2. The threshold temperature for enabling the output again and resetting the latch after OTP has been activated.

Typical Performance Characteristics

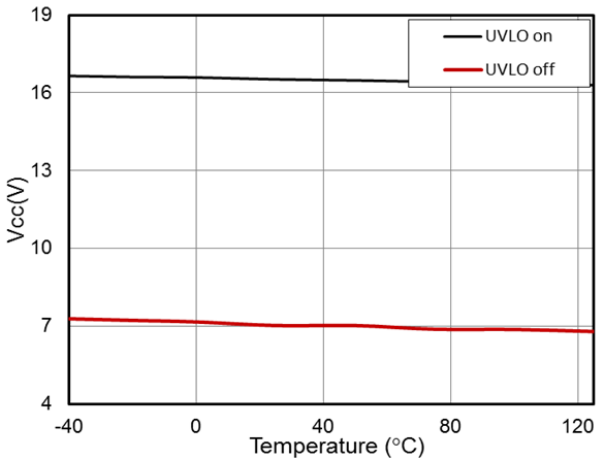


Fig 3. UVLO Level vs. Temperature

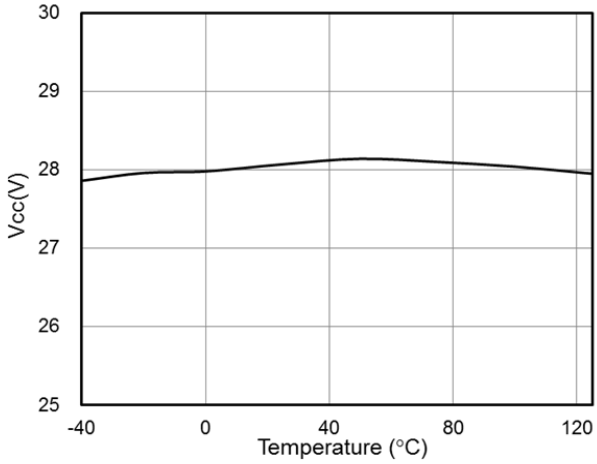


Fig 4. Vcc OVP Level vs. Temperature

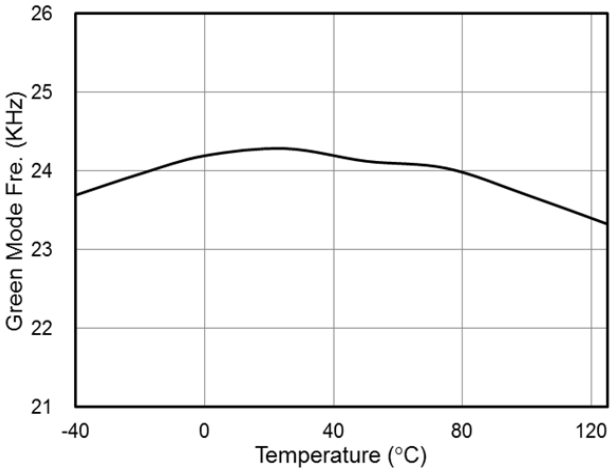


Fig 5. Green Mode Fre. vs. Temperature

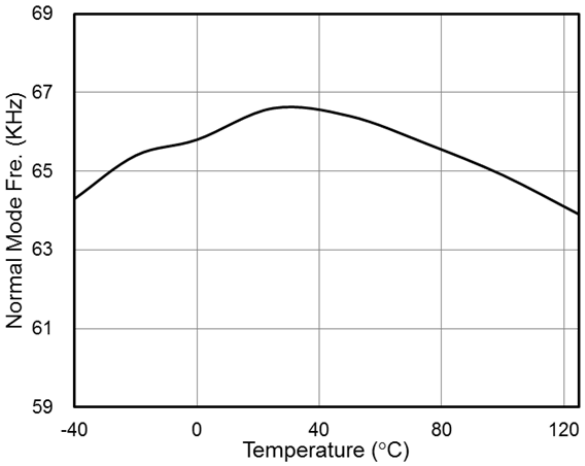


Fig 6. Normal Mode Fre. vs. Temperature

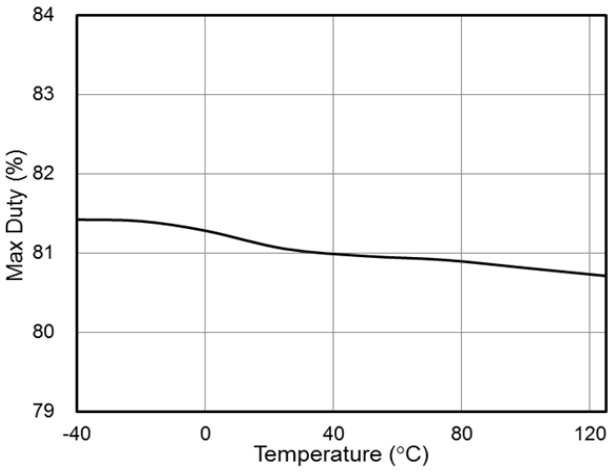


Fig 7. Max Duty vs. Temperature

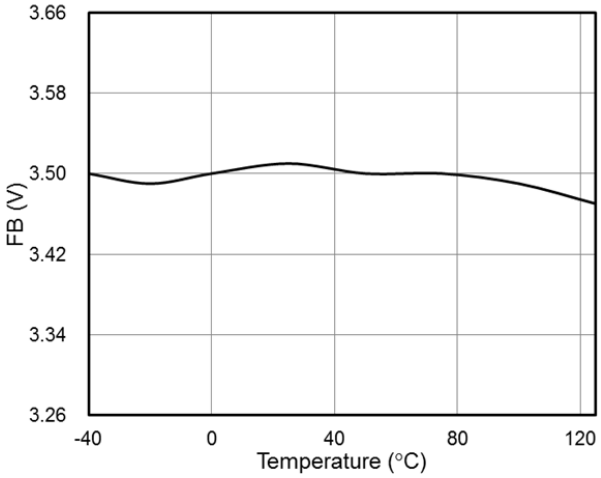


Fig 8. FB OVP Level vs. Temperature

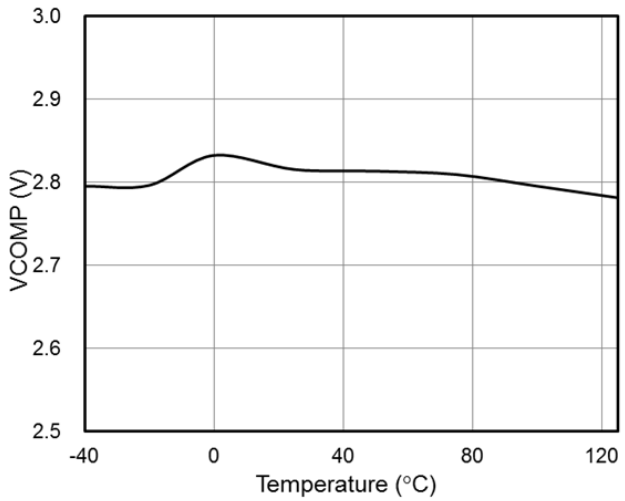


Fig 9. VOLP Level vs. Temperature

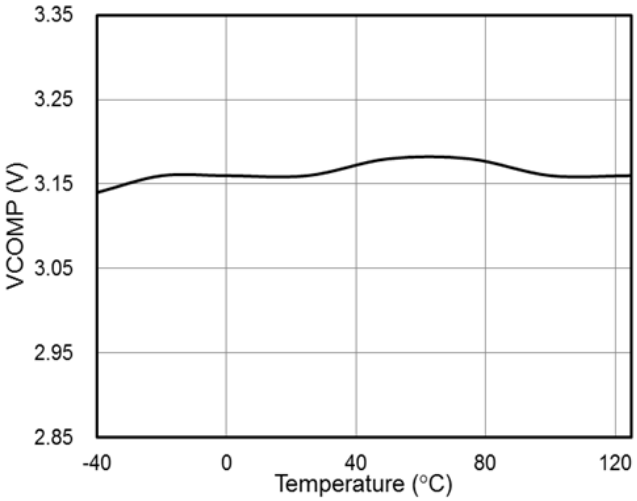


Fig 10. Open Loop Voltage vs. Temperature

Application Information

Operation Overview

The LD9535K is built in a multi-mode PWM controller and integrated a 650V MOSFET. The LD9535K operates a constant frequency to achieve the CCM as heavy load. For demanding higher power efficiency and power-saving in light load condition, the LD9535K implements QR function to allow the valley switching and accomplish zero voltage switching (ZVS). Under different load conditions, LD9535K provides the different solutions for achieving higher efficiency and performance.

Under Voltage Lockout (UVLO)

An UVLO comparator is implemented in it to detect the voltage on the VCC pin. It would assure the supply voltage enough to turn on the LD9535K. As shown in Fig. 11, a hysteresis is built in to prevent the shutdown from the voltage dip during startup. The turn-on and turn-off threshold level are set at 16.5V and 7V, respectively.

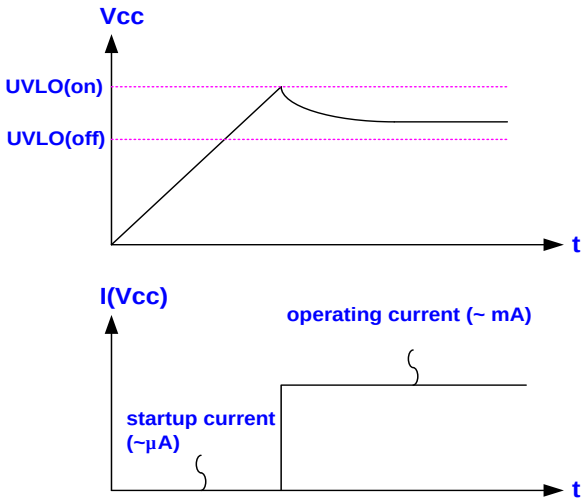


Fig. 11

Startup Current and Startup Circuit

The typical startup circuit to generate the LD9535K VCC is shown in Fig. 12. During the startup transient, the VCC is lower than the UVLO threshold thus LD9535K will not to turn on. Therefore, the current through R1 will provide the startup current and to charge the capacitor C1. Whenever the VCC voltage is high enough to turn on the LD9535K the supply current is provided from the auxiliary winding of the transformer.

Lower startup current requirement on the PWM controller will help to increase the value of R1 and then reduce the power consumption on R1. By using CMOS process and the special circuit design, the maximum startup current of LD9535K is only 1μA. If a higher resistance value of R1 is chosen, it usually takes more time to start up. To select the value of R1 and C1 carefully will optimize the power consumption and startup time.

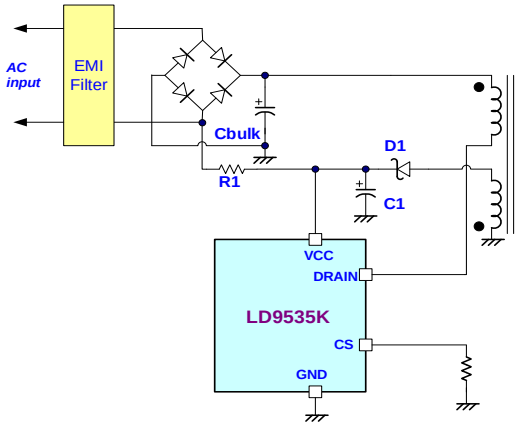


Fig. 12

QR Mode Detection

The transformer will be demagnetized after the main power MOSFET turns off. A quasi resonant signal will be detected from auxiliary winding by FB pin through the external resister.

As soon as the current of the secondary side diode is down to zero during MOSFET-off period, the transformer's core is demagnetized completely. V_{DS} of MOSFET will resonate in discontinuous current mode.

The resonance frequency (F_{QR}) will be obtained as below.

$$F_{QR} = \frac{1}{2\pi\sqrt{L_m * C_R}} (HZ)$$

L_M = Inductance of primary winding

C_R = Resonance equivalent parasitic capacitance

If V_{DS} voltage falls to resonant valley level from max plateau value, the QRD comparator will be tripped while FB pin current is close to 20μA.

However, the QR detection will be influenced by propagation delay. If inductance of primary winding is less than 500μH, there is barb in Vds (as shown in Fig. 13).

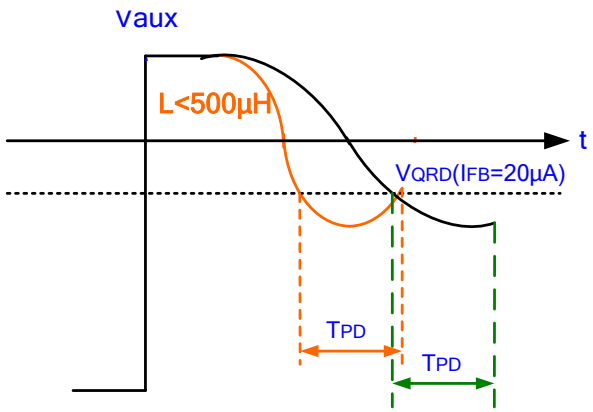


Fig. 13

Voltage Feedback Loop

The voltage feedback signal is provided from the TL431 at the secondary side through the photo-coupler to the COMP pin of the LD9535K. Similar to UC3842, the LD9535K would without voltage offset to feed the voltage divider at the ratio of RA and RB, that is,

$$V_{-(PWM_{COMPARATOR})} = \frac{RB}{RA + RB} \times V_{COMP}$$

A pull-high resistor is embedded internally and therefore no external one is required.

The LD9535K integrates the multi-mode PWM controller, and for enhance the light load efficiency, the comp pin value corresponding to the frequency is as shown in Fig. 14.

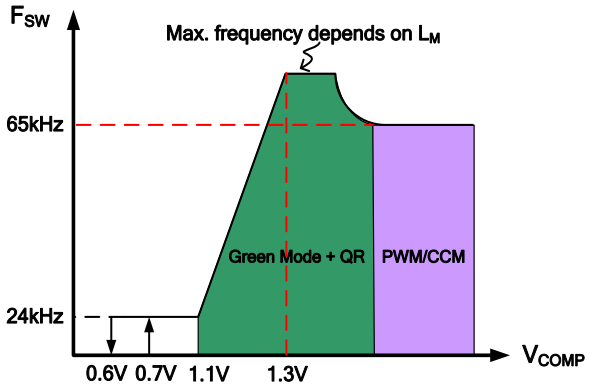


Fig. 14

Current Sensing, Leading Edge Blanking

The typical current mode of PWM controller feedbacks both current signal and voltage signal to close the control loop and achieve regulation. The LD9535K detect the primary MOSFET current from the CS pin, which is not only for the peak current mode control but also for the pulse-by-pulse current limit. The maximum voltage threshold of the current sensing pin sets at 0.5V. From above, the MOSFET peak current can be obtained from below.

$$I_{PEAK(MAX)} = \frac{0.5V}{R_{CS}}$$

A leading-edge blanking (LEB) timer is included in the input of CS pin to prevent false trigger from the turn-on current spike (as shown in Fig. 15).

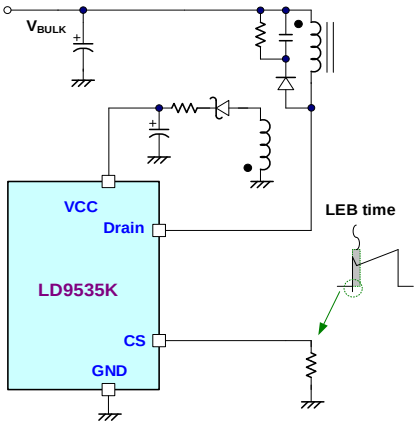


Fig. 15

CCM Switching Frequency Clamp

According to the QR operation principle, the switching frequency is inversely proportional to the output power. Therefore, as the output power increases, the switching frequency can become rather low without limiting. The CCM switching frequency of LD9535K is clamped at 65 kHz internally to provide the optimized operations by considering the EMI performance, thermal treatment, component sizes and transformer design.

Over Voltage Protection on VCC Pin (VCC OVP) – Auto Recovery

LD9535K is implemented with an OVP function on VCC. Whenever the VCC voltage is higher than the OVP threshold voltage, the LD9535K will be shutdown simultaneously thus to stop the switching of the power MOSFET until the next UVLO(ON).The VCC OVP function in LD9535K is an auto-recovery type protection. The Fig. 16 shows its operation.

On the other hand, if the OVP condition is removed, the VCC level will get back to normal level and the output will automatically return to the normal operation.

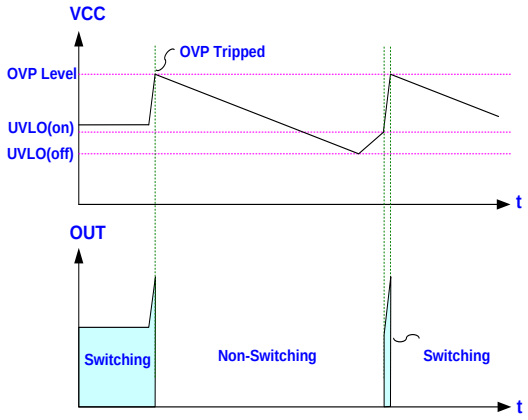


Fig. 16

Over Load Protection (OLP) – Auto Recovery

To protect the circuit from damage due to over-load condition and short or open-loop condition, the LD9535K is implemented with smart OLP function. It also features auto – recovery function, see Fig. 17 for the waveform. In case of fault condition, the feedback system will force the voltage loop toward the saturation and then pull the voltage high on COMP pin (VCOMP). When the V_{COMP} ramps up to the OLP threshold of 2.8V and continues over OLP delay time, the protection will be activated and then turn off the gate output to stop the switching of power circuit.

With the protection mechanism, the average input power will be minimized to remain the component temperature and stress within the safe operating area.

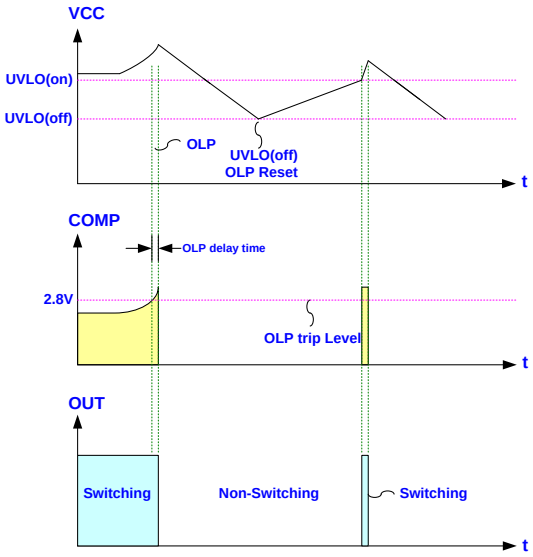


Fig. 17

Brown-In/ Brown-Out Protection (BNI/BNO) and Bulk Cap OVP – Auto Recovery

The LD9535K integrates the brown in/out and bulk cap protections and valley detection into FB pin. The auxiliary voltage reflects a proportional bulk voltage during the on time. Fix the internal current at the BNI and BNO, the BNI level could be set by modulating the FB divided resistors and auxiliary voltage, as shown in Fig. 18. For preventing the abnormal condition of line voltage to causing damage, BNO function is implemented, while turns off the gate signal after de-bounce time 75ms as BNO occurring, as shown in

Fig. 19. The relationship of input voltage and BNI/BNO is expressed in following equation.

$$V_{DC\_BNI} = \frac{N_P}{N_a} \cdot I_{BNI} \cdot R_1$$

$$V_{DC\_BNO} = \frac{N_P}{N_a} \cdot I_{BNO} \cdot R_1$$

$$V_{DC\_BULK\_OVP} = \frac{N_P}{N_a} \cdot I_{BULK\_OVP} \cdot R_1$$

, where

V_{DC_BNI} is predicted BNI DC value of input voltage.

V_{DC_BNO} is predicted BNO DC value of input voltage.

$V_{DC\_BNULK\_OVP}$ is predicted BULK OVP DC value of input voltage.

I_{BNI} is BNI trip current.

I_{BNO} is BNO trip current.

I_{BULK_OVP} is BULK OVP trip current.

N_p is turns ration of primary-side winding.

N_a is turns ration of auxiliary winding.

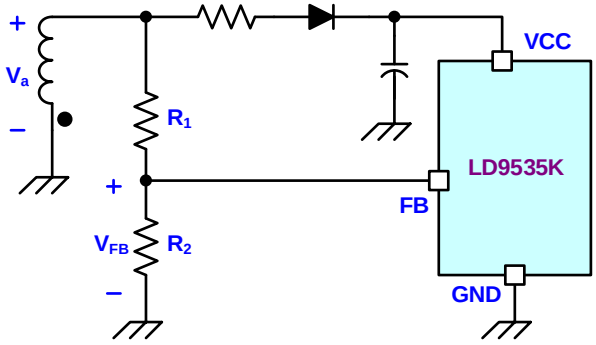


Fig. 18

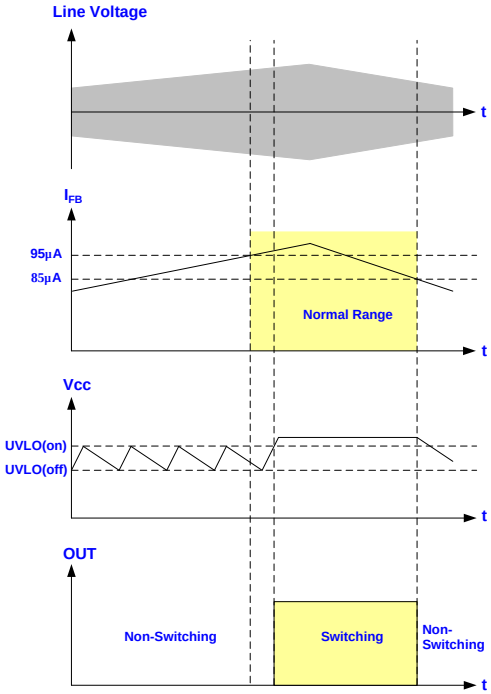


Fig. 19

Over Voltage Protection on FB Pin (FB OVP) – Auto Recovery

An output overvoltage protection is implemented in the LD9535K. The auxiliary winding voltage can be reflected from secondary winding, in which the FB pin voltage is proportional to output voltage during the gate off time. OVP is worked by sensing the auxiliary voltage via the divided resistors R2, refereeing to Fig. 18. The equation of FB OVP is shown as follows.

$$R_2 = \frac{R_1 \cdot V_{FB\_OVP}}{V_a - V_{FB\_OVP}}$$

$$V_a = \frac{N_a}{N_S}(V_O + V_F)$$

V_{FB_OVP} is the FB pin OVP trip voltage level. V_a is the auxiliary winding voltage which reflects from the forward voltage V_F of Schottky diode and output voltage V_O. N_S is turns ration of secondary-side winding.

If V_{FB} overs the FB OVP trip level, the internal counter starts counting 8 cycles, and then LD9535K goes to

auto-recovery protection mode till the FB OVP status is defused.

Output Short Circuit Protection (OSCP) – Auto Recovery

The OSCP function can prevent the damage from output short circuit. Once the output is shorted, Vo and V_{CC} drop immediately, which always reflects the auxiliary winding during the gate off region. Therefore, as V_{FB} is lower than 0.8V during gate off region, then the FB_UVP is triggered, and skips one cycle. According to the close loop control, COMP voltage will pull high in the meanwhile. If the VCOMP pulls higher than 2.8V over 15 ms and Vcc drops below 9.6V. At this time, the OSCP protection will be triggered and turn off the gate driving.

Oscillator and Switching Frequency

The LD9535K is implemented with frequency swapping function which helps the power supply designers to both optimize EMI performance and lower system cost.

Green Mode Operation

By using the green-mode control, the switching frequency can be reduced under the light load condition. This feature helps to improve the efficiency in light load conditions. The green-mode control is Leadtrend Technology's own property.

Fault Protection

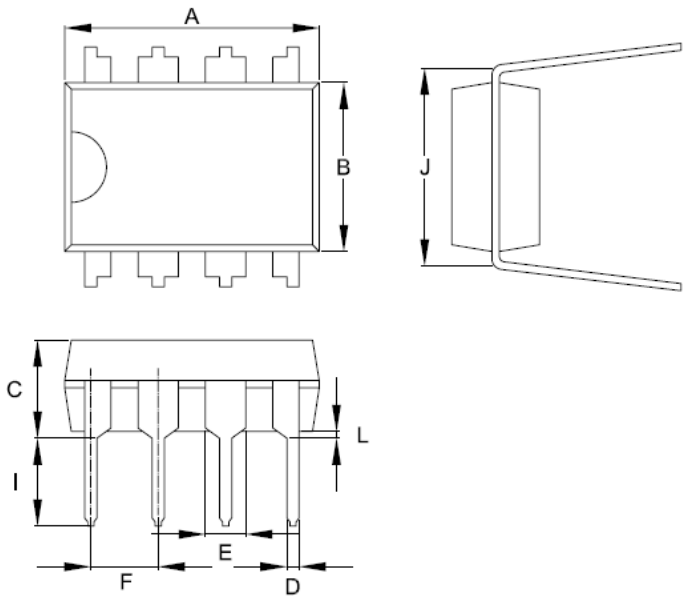
There are several critical protections integrated in the LD9535K to prevent from damage to the power supply. Those damages usually come from open or short conditions on the pins of LD9535K.

In case under such conditions listed below, the gate output will turn off immediately to protect the power circuit.

1. CS pin floating
2. COMP pin floating

Package Information

DIP-8



Symbol	Dimension in Millimeters		Dimensions in Inches	
	Min	Max	Min	Max
A	9.017	10.160	0.355	0.400
B	6.096	7.112	0.240	0.280
C	-----	5.334	------	0.210
D	0.356	0.584	0.014	0.023
E	1.143	1.778	0.045	0.070
F	2.337	2.743	0.092	0.108
I	2.921	3.556	0.115	0.140
J	7.366	8.255	0.29	0.325
L	0.381	------	0.015	------

Revision History

REV.	Date	Change Notice
00	10/12/2020	Original Specification