Leadtrend 通嘉科技

LD5762P

05/02/2017

High Voltage Multi-Mode PWM Controller with BNO Function

REV. 00

General Description

The LD5762P is a green-mode PWM IC built-in with brown-in/ out functions in a SOP-7/SOP-8 package. The device could therefore minimize the component counts, circuit space, and reduces the overall material cost of power applications.

The LD5762P features HV start, sleep-mode, green-mode power-saving operation, and internal slope compensation, soft-start functions which could minimum the power loss and improve the system performance.

With complete protection with it, like OPP (Over Power Protection), OVP (Over Voltage Protection), OCP (Over Current protection) and brown-in/out protection, LD5762P prevents the circuit from being damaged in abnormal conditions.

Furthermore, the LD5762P features frequency swapping and soft driving function to minimize the noise and improve EMI.

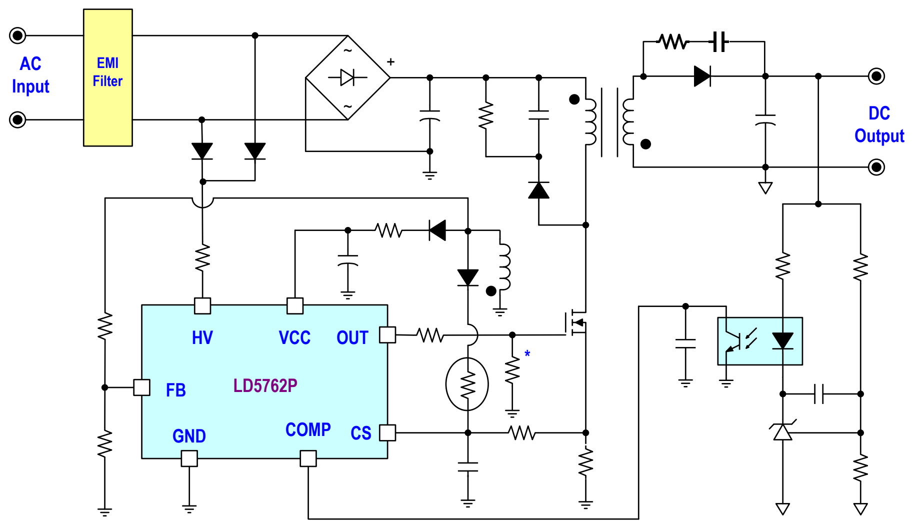
Features

- Secondary-side feedback control with quasi-resonant + CCM operation
- High-Voltage (710V) Startup Circuit
- Built-in Brown-in/out Function on HV pin
- Built- in X-Cap Discharge on HV pin
- OVP (Over Voltage Protection) on VCC/FB
- OPP (Over Power Protection)
- OCP (Over Current Protection)
- OSCP(Output Short Circuit Protection)
- Adj. CS_OTP (Over Temperature Protection)
- Peak Load FSW Boost
- Soft Driving
- +300mA/-800mA Driving Capability

Applications

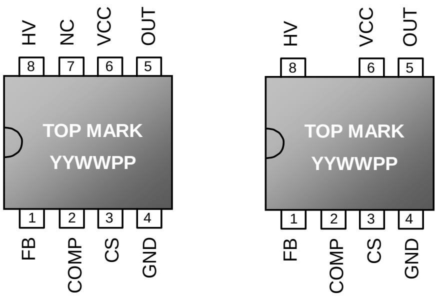
- Printer

Typical Application



Pin Configuration

SOP-8 (TOP VIEW) SOP-7 (TOP VIEW)



YY: Year code
WW: Week code
PP: Production code

Ordering Information

Part number	Package	Top Mark	Shipping
LD5762P GS	SOP-8	LD5762PGS	2500 /tape & reel
LD5762P GR	SOP-7	LD5762PGR	2500 /tape & reel

The LD5762P is RoHs compliant/ Green Packaged.

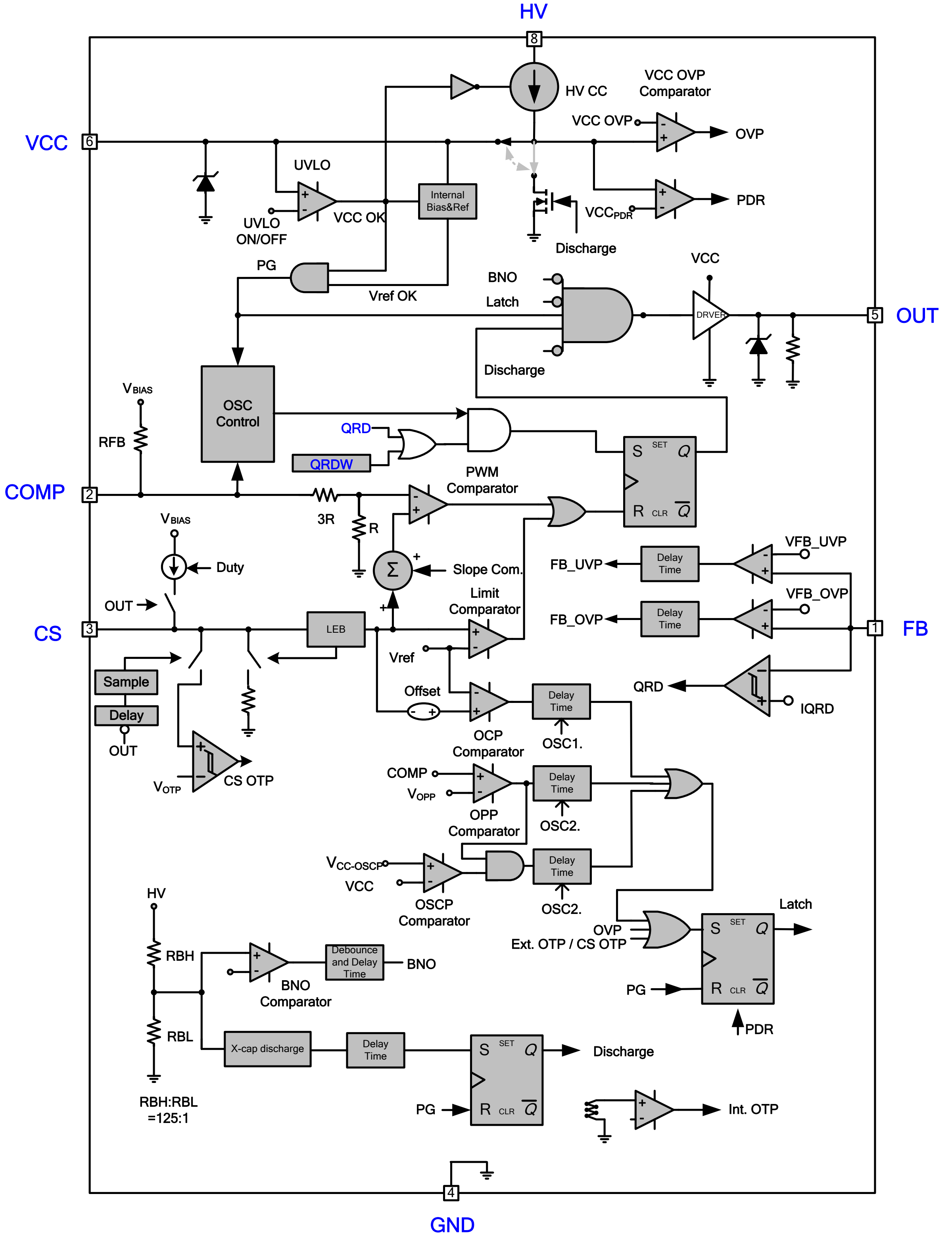
Protection Mode

Part number	VCC_OVP	OSCP	CS_OTP	OPP	FB_UVP	FB_OVP
LD5762P	Latch	Latch	Latch	Latch	Skip 1 cycle	Latch

Pin Descriptions

PIN	NAME	FUNCTION
1	FB	Auxiliary voltage sense, output voltage protection and quasi resonant detection.
2	COMP	Voltage feedback pin. Connect a photo-coupler with it to close the control loop and achieve the regulation.
3	CS	Current sense pin, connect it to sense the MOSFET current
4	GND	Ground
5	OUT	Gate drive output to drive the external MOSFET
6	VCC	Supply voltage pin
7	NC	Unconnected Pin
8	HV	Connect this pin to Line/ Neutral of AC main voltage through resistor to provide the startup current for the controller. When VCC voltage increase to trip the point of $UVLO_{(ON)}$, this HV loop will be turned off to reduce the power loss on the startup circuit. An internal resistor divider between HV to GND pin will monitor AC line voltage to activate Brown-in/out function control.

Block Diagram



Absolute Maximum Ratings

Supply Voltage VCC	-0.3V~33V
HV	-0.3V~710V
COMP, FB, CS	-0.3V~6V
OUT	-0.3V~VCC+0.3V
Maximum Junction Temperature	150°C
Storage Temperature Range	-65°C to 150°C
Package Thermal Resistance (SOP-8/SOP-7)	160°C/W
Power Dissipation (SOP-8/SOP-7, at Ambient Temperature = 85°C)	250mW
Lead temperature (Soldering, 10sec)	260°C
ESD Voltage Protection, Human Body Model (except of HV Pin)	2.5KV
ESD Voltage Protection, Machine Model (except of HV Pin)	250V
ESD Voltage Protection, Human Body Model (HV Pin)	1KV
ESD Voltage Protection, Machine Model (HV pin)	200V
Gate Output Current	+300/-800mA

Caution:

Stress exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stress above Recommended Operating Conditions may affect device reliability.

Recommended Operating Conditions

Item	Min.	Max.	Unit
Operating Junction Temperature	-40	125	°C
Supply VCC Voltage	8.5	26.5	V
HV resistor Value (AC Side)	8	17.5	KΩ
HV to GND Capacitor Value	--	300	pF
Comp Pin Capacitor	1	10	nF
CS Pin Capacitor Value	47	390	pF

Electrical Characteristics

(T_A = +25°C unless otherwise stated, VCC=15.0V)

PARAMETER	CONDITIONS	SYMBOL	MIN	TYP	MAX	UNITS
High-Voltage Supply (HV Pin)						
High-Voltage Current Source	VCC< $UVLO_{(ON)}$, HV=500V_{DC}	I_{HV}	2	2.8	3.5	mA
HV Discharge capability	HV=500V_{DC}	I_{HV_DIS}	2	2.5	3.5	mA
HV Pin Total Input Current (HV+ BNO)	*HV= 500V_{DC},VCC> $UVLO_{(ON)}$,	I_{HV_LEAK}			35	μA
HV Pin Brown-In Level (HVBI)	HV pin =half rectifier wave increase	V_{HVBO}	90	100	110	V_{DC}
HV Pin Brown-out Level(HVBO)	HV pin = half rectifier wave decrease	V_{HVBI}	72	82	92	V_{DC}
HV Pin BNO Hysteresis	HV_{BI}-HV_{BO}	ΔV_{HV}	7	16	23	V_{DC}
Brown-in De-bounce Time	*V_{COMP}=3V	T_{D_HVBI}		300		μs
Brown-out Detection Delay time	V_{COMP}=3V	T_{D_HVBO}	52	65	78	ms
HV Pin Min. Operation Voltage	*VCC=15V (DetVmin = VHV-VCC = 30V)	V_{HV_MIN}	45			V
X-Cap discharge Detection Delay time	V_{COMP}=3V	T_{D_XCAP}	52	65	78	ms
Supply Voltage (VCC Pin)						
Startup Current	VCC=15V,HV=500V_{DC}	I_{CC_ST}		25	50	μA
Operating Current (with 1nF load on OUT pin)	V_{COMP}=3V	I_{CC_OP1}	1.5	2	2.5	mA
	V_{COMP}=0V	I_{CC_OP2}	0.3	0.33	0.45	mA
	Latch mode	I_{CC_OPL}	0.35	0.43	0.55	mA
	Auto mode	I_{CC_OPR}	0.25	0.28	035	mA
$UVLO_{(OFF)}$		$VCC_{\_OFF}$	5.5	6	6.5	V
$UVLO_{(ON)}$		$VCC_{\_ON}$	15	16	17	V
PDR	*	$VCC_{\_PDR}$		$UVLO_{(OFF)}$-1.1V		V
VCC HVBI Level	*HV>HVBI	$VCC_{\_HVBI}$		$UVLO_{(OFF)}$+4V		V
VCC OVP Level		$VCC_{\_OVP}$	31	32	33	V
VCC OVP De-bounce Time	V_{COMP}=3V	T_{D_VCCOVP}	50	120	250	μs

PARAMETER	CONDITIONS	SYMBOL	MIN	TYP	MAX	UNITS
Oscillator for Switching Frequency						
Frequency	V_{COMP}=3V	F_{SW_N}	61	65	69	kHz
	V_{COMP}=4.4V	F_{SW_H}	115	130	140	kHz
Green Mode Frequency	With fsw swapping	F_{SW_GREEN}	22	25	28	kHz
Trembling Frequency	Frequency= 25kHz	F_{TRM1}	±2	±4	±6	kHz
	Frequency= 65kHz	F_{TRM2}	±3	±6	±9	kHz
	Frequency=130kHz	F_{TRM3}	±7	±10	±13	kHz
Modulation Frequency	*	F_{SW_MOD}		200		Hz
F_{SW} Temp. Stability	-40°C ~105°C	F_{SW_TS}	0	3	4	%
F_{SW} Voltage Stability	VCC=8V-(OVP-1V)	F_{SW_VS}	0		1	%
Maximum On Time		DMAX	75	80	85	%
OSCP (Output Short Circuit Protection)						
OSCP Trip Level	*	$VCC_{\_OSCP}$		$UVLO_{OFF}$ +4V		V
OSCP Delay Time	*	T_{D_OSCP}		10		ms
Voltage Feedback (Comp Pin)						
Input Voltage to Current-Sense Attenuation	*	A_V		1/4.0		V/V
Comp Impedance		Z_{COMP}	37	42	47	kΩ
Open Loop Voltage	COMP pin open	V_{COMP_OPEN}	4.9	5.2	5.5	V
OPP Tripped Level	TC: track COMP pin open voltage	V_{OPP}	4.4	4.6	4.8	V
Zero Duty Threshold VCOMP on Burst mode	Zero Duty (Fig 1.)	V_{ZDC}	1.85	1.95	2.05	V
	Hysteresis	V_{ZDCH}	50	110	150	mV

PARAMETER	CONDITIONS	SYMBOL	MIN	TYP	MAX	UNITS
Current Sensing (CS Pin)						
Limit Voltage	Vsetting<0.15V	V_{CS_MAX1}	0.85	0.875	0.90	V
	Vsetting>0.15V	V_{CS_MAX2}	0.80	0.825	0.85	V
OCP Voltage for Low line	VFB>1.5V	V_{CS_L1}	0.55	0.575	0.60	V
	VFB<1.5V	V_{CS_L2}	0.395	0.425	0.455	V
OCP Voltage for High line	VFB>1.5V	V_{CS_H1}	0.51	0.535	0.56	V
	VFB<1.5V	V_{CS_H2}	0.355	0.385	0.415	V
OPP Compensation Current	Duty=50%	I_{OPP_50}	15	25	40	μA
	Duty=20%	$I_{OPP\_20\_H}$	285	300	315	μA
IOPP Threshold VCOMP	Duty=20%	V_{IOPP}	3.7	3.9	4.1	V
OCP Delay Time		T_{D_OCP}	1.4	1.7	2.0	s
OCP Reset Time	*	T_{D_OCPRS}		2		ms
Leading Edge Blanking Time		T_{LEB}	200	300	400	ns
Delay to Output		T_{PD}	50	70	150	ns
Slope Compensation Level	*	V_{SLP_L}	0		0.156	V
Slope Compensation Position	*	V_{SLP}	0		80	%
Gate Drive Output (OUT Pin)						
Output Low Level	VCC=15V, Io=20mA	V_{OL}	0		1	V
Output High Level	VCC=15V, Io=20mA	V_{OH}	8		VCC	V
Rising Time	Load Capacitance= 1000pF	T_r	30	90	120	ns
Falling Time	Load Capacitance= 1000pF	T_f	5	20	30	ns
OUT Pin Clamping Voltage	VCC= 21V,1nF on OUT pin	V_{O_CLAMP}	16	18	20	V
OPP (Over Power Protection)						
OPP Delay Time		T_{D_OPP}	260	320	380	ms

PARAMETER	CONDITIONS	SYMBOL	MIN	TYP	MAX	UNITS
QRD (Quasi Resonant Detection, FB Pin)						
UVP Trip voltage Level	(VHV> $250V_{DC}$)	V_{FB_UVP}	0.45	0.5	0.55	V
De-bounce Cycle	*(VHV> $250V_{DC}$)	T_{SKIP}		1		Cycle
OVP Trip voltage Level		V_{FB_OVP}	2.85	3	3.15	V
De-bounce Cycle	*	T_{D_FBOVP}		8		Cycle
QRD Trip Level	*	I_{QRD}		20		μA
QRD Delay Time	*	T_{QRD}		100		ns
Soft Start						
Soft Start Duration(1)	After OPP, OCP, OTP, BNO, OVP is tripped	T_{SS1}	4	6	8	ms
Soft Start Duration(2)	*Fsw=65kHz	T_{SS2}	30			ms
Internal OTP						
OTP Tripped Level(T_{OTP})	*	T_{INOTP}		140		°C
OTP Hysteresis	*	T_{INOTP_HYS}		T_{OTP}-30		°C
OTP De-bounce Time	*	T_{D_INOTP}		50		μs
CS_OTP (Over Temperature Protection Protection)						
OTP Trip Current Level	VFB>1.5V	V_{CSOTP1}	0.425	0.45	0.475	V
	VFB<1.5V	V_{CSOTP2}	0.125	0.15	0.175	V
VCS Discharge Time	*Gate On (Ron=350ohm)	T_{DIS_CS}		LEB		ns
De-bounce Time	V_{COMP}=3V	T_{D_CSOTP}	20	35	50	ms

*: Guaranteed by design

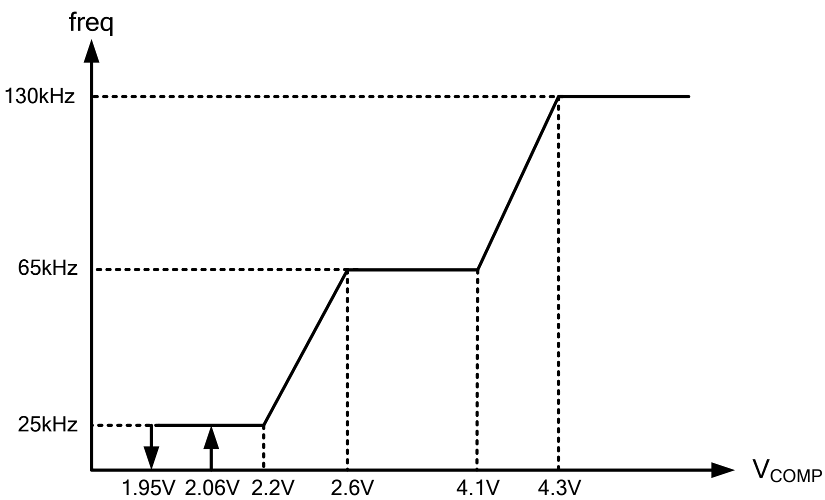


Fig. 1 V_{COMP} vs. PWM Frequency

Typical Performance Characteristics

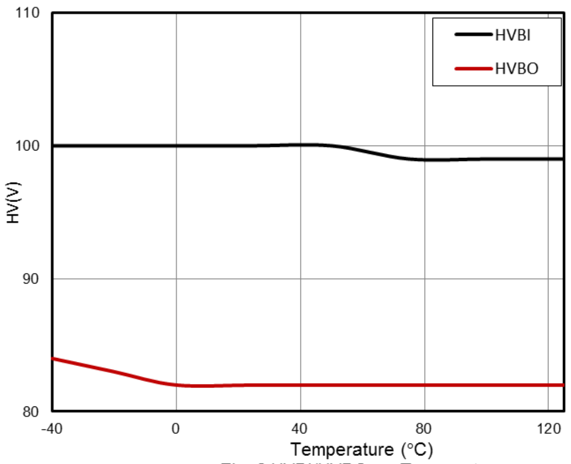


Fig. 2 HVBI/HVBO vs.Temperature

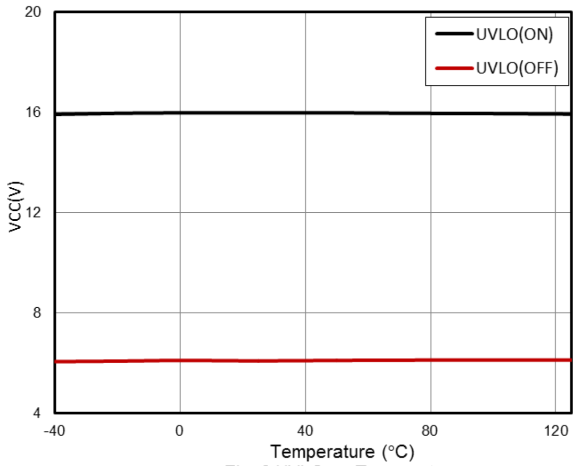


Fig. 3 UVLO vs.Temperature

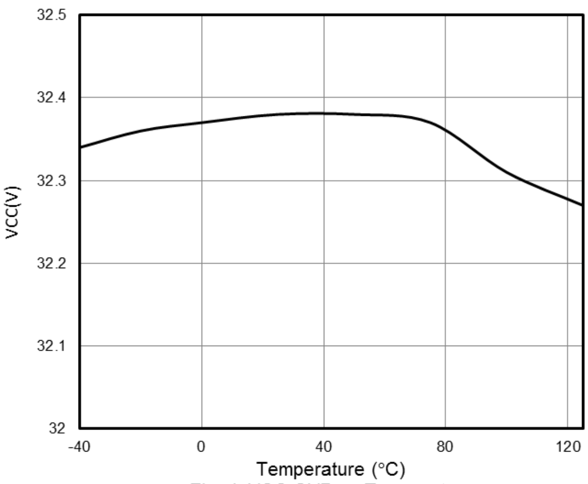


Fig. 4 VCC OVP vs.Temperature

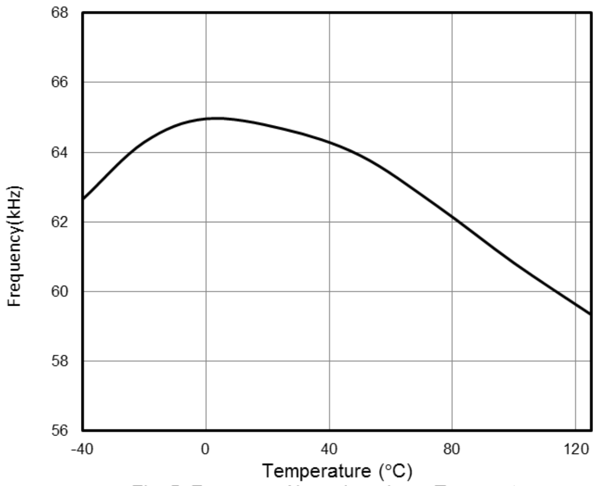


Fig. 5 Frequency Normal mode vs.Temperature

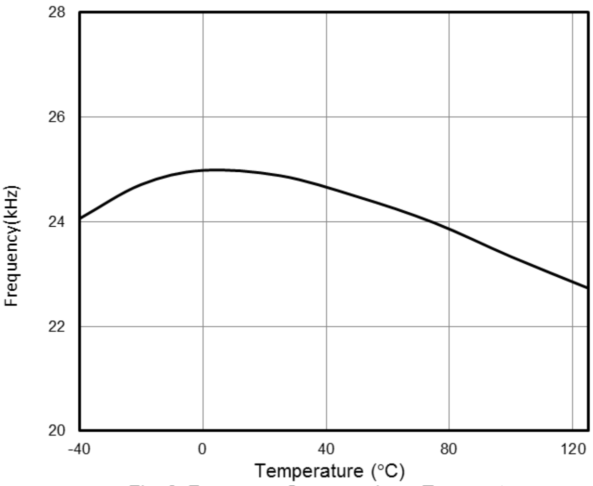


Fig. 6 Frequency Green mode vs.Temperature

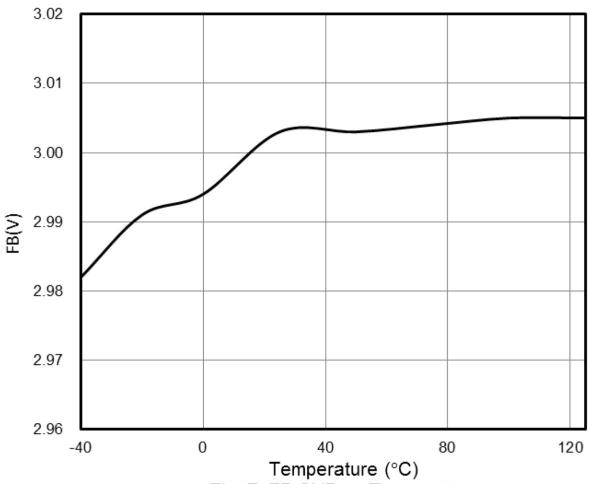


Fig. 7 FB OVP vs.Temperature

Application Information

Operation Overview

As long as the green power requirement becomes a trend and the power saving is getting more and more important for the switching power supplies and switching adaptors, the traditional PWM controllers are not able to support such new requirements. Furthermore, the cost and size limitation force the PWM controllers to be more powerful and with more functions to reduce the external part counts. The LD5762P is ideal for these applications. Its detailed features are described as below.

Internal High-Voltage Startup Circuit and Under Voltage Lockout (UVLO)

The traditional circuit provides the startup current through a startup resistor to power up the PWM controller. However, it consumes much significant power to meet the current power saving requirement. In most cases, startup resistors carry larger resistance and spend more time to start up.

To achieve the optimized topology, as shown in Fig. 8, LD5762P is implemented with a high-voltage startup circuit for such requirement. At startup, the high-voltage current source sinks current of AC Line/or Neutral to provide startup current and charge the capacitor C1 connected to VCC.

During the startup transient, the HV current will supply around 2.8mA to VCC capacitor until this VCC voltage reaches the UVLO threshold VCC. By using such configuration, the turn-on delay time will be almost same no matter under low-line or high-line conditions.

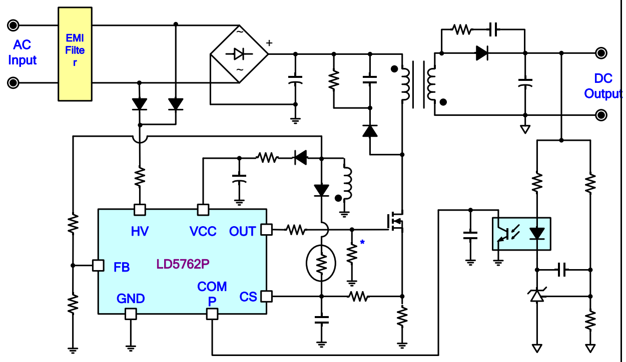


Fig. 8

As VCC trips $UVLO_{(OFF)}$, HV pin will recharge VCC capacitor till VCC voltage rises back to $UVLO_{(ON)}$ again. Since then, HV pin would no longer charge the capacitor and instead, send a gate drive signal to draw supply current for VCC from the auxiliary winding of the transformer. That minimizes the power loss on the start-up circuit successfully.

An UVLO comparator is embedded to detect the voltage across the VCC pin to ensure the supply voltage enough to power on the LD5762P and in addition, to drive the power MOSFET. As shown in Fig. 9, a hysteresis is provided to prevent shutdown from the voltage dip during startup. The turn-on and turn-off threshold level are set at 16V and 6V, respectively.

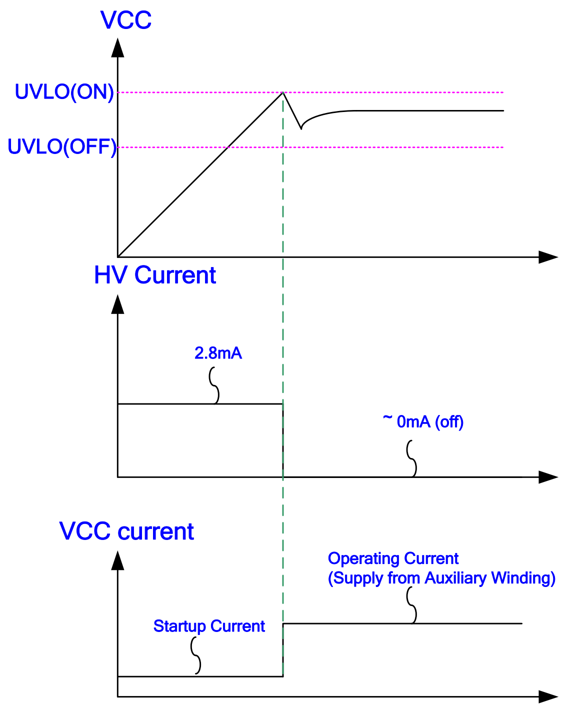


Fig. 9

QR Mode Detection

The transformer will be demagnetized after the main power MOSFET turns off. A quasi resonant signal will be detected from auxiliary winding by FB pin through the external resister.

As soon as the current of the secondary side diode is down to zero during MOSFET-off period, the transformer's core is demagnetized completely. V_{DS} of MOSFET will resonate in discontinuous current mode. The resonance frequency (F_{QR}) will be obtained as below.

$$F_{QR} = \frac{1}{2\pi\sqrt{L_m \times C_R}} (Hz)$$

L_M = Inductance of primary winding

C_R = Resonance equivalent parasitic capacitance

If V_{DS} voltage falls to resonant valley level from max plateau value, the QRD comparator will be tripped while FB pin current is close to 20μA.

Brown in/out Protection

The LD5762P features Burn-in/out function on HV pin. As the built-in comparator detects the half wave rectify line voltage condition, it will shut off the controller to prevent from any damage. Fig. 10 shows the operation. When V_{HV} < HVBO, the gate output will remain off even when the VCC already reaches $UVLO_{(ON)}$. It therefore forces the VCC hiccup between $UVLO_{(ON)}$ and $UVLO_{(OFF)}$. Unless the line voltage rises over HVBI V_{AC}, the gate output will not start switching even as the next $UVLO_{(ON)}$ is tripped. A hysteresis is implemented to prevent the false-triggering during turn-on and turn-off.

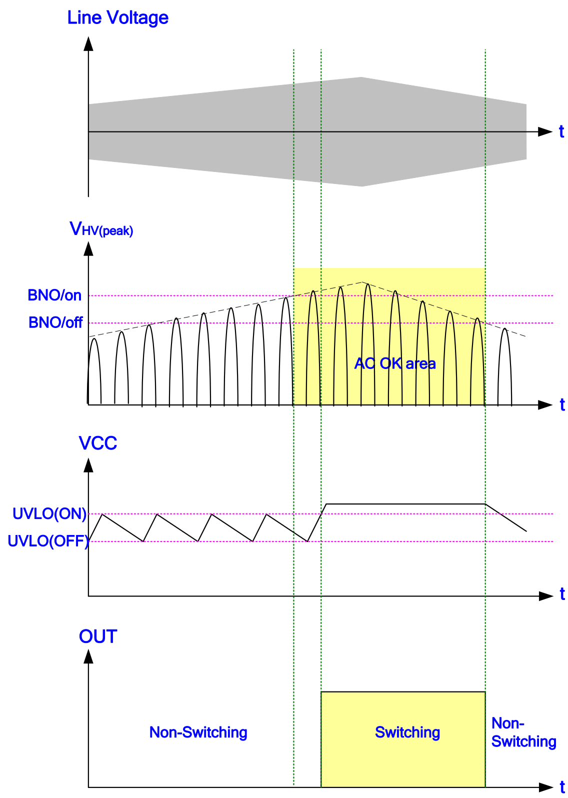


Fig. 10

Current Sensing, Leading-Edge Blanking and the Negative Spike on CS Pin

The typical current mode PWM controller feedbacks both current signal and voltage signal to close the control loop and achieve regulation. The LD5762P detects the primary MOSFET current across CS pin to control in peak current mode and also limit the pulse-by-pulse current. The maximum voltage threshold of the current sensing pin sets at 0.875V (Vsetting<0.15V). Thus the MOSFET peak current can be calculated as:

$$I_{PEAK(MAX)} = \frac{0.875V}{R_S}$$

A 300ns leading-edge blanking (LEB) time is designed in the input of CS pin to prevent false-triggering from the current spike. In the low power applications, if the total pulse width of the turn-on spikes is less than 150ns and the negative spike on the CS pin does not exceed -0.3V, the R-C filter (as shown in Fig. 11) is free to eliminate.

However, the total pulse width of the turn-on spike is related to the output power, circuit design and PCB layout. It is strongly recommended to add a small R-C filter (as shown in Fig. 12) for larger power application to avoid the CS pin from being damaged by the negative turn-on spike.

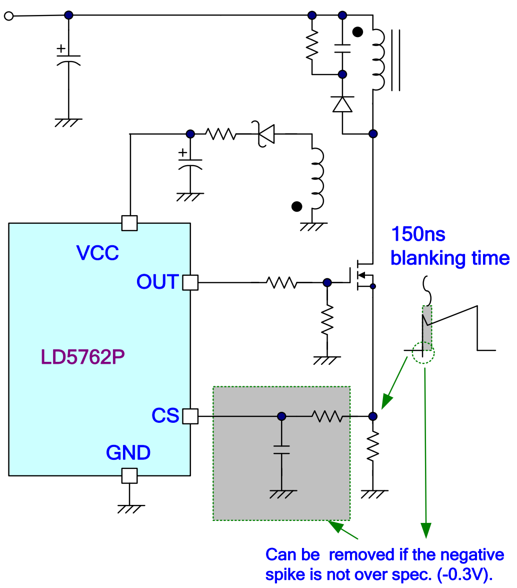


Fig. 11

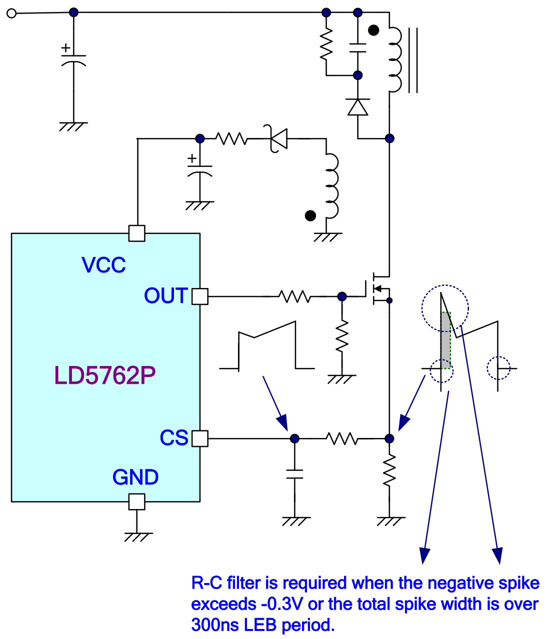


Fig. 12

Output Stage and Maximum Duty-Cycle

An output stage of a CMOS buffer with typical 300mA driving capability is incorporated to drive a power MOSFET directly. The maximum duty-cycle of LD5762P is limited to 80% to avoid the transformer saturation.

Voltage Feedback Loop

The voltage feedback signal is provided from the TL431 on the secondary side through the photo-coupler to the COMP pin of LD5762P. Similar to UC384X, its input stage is with 1 diodes voltage offset to feed the voltage divider with 1/4 ratio, that is,

$$V_{cs(PWM_{COMPARATOR})} = \frac{1}{4} \times V_{COMP}$$

A pull-high resistor is embedded internally to optimize the external circuit.

Internal Slope Compensation

A fundamental issue of current mode control is the stability problem when its duty-cycle is operated for more than 50%. To stabilize the control loop, the slope compensation is required in the traditional UC384X design by injecting the ramp signal from the RT/CT pin through a coupling capacitor. LD5762P has internal slope compensation circuit to simplify the external circuit design.

Oscillator and Switching Frequency

The LD5762P has the switching frequency between 65 kHz ±6kHz internally to optimize its performance in EMI, thermal treatment, component sizes and transformer design.

Dual-Oscillator Green-Mode Operation

There are many different topologies has been implemented in different chips for the green-mode or power saving requirements such as “burst-mode control”, “skipping-cycle mode”, “variable off-time control “…etc. The basic operation theory of all these approaches intended to reduce the switching cycles under light-load or no-load condition either by skipping some switching pulses or reduce the switching frequency.

By using LD proprietary dual-oscillator technique, the green-mode frequency can be well controlled and further to avoid the generation of audible noise.

Frequency Swapping

The LD5762P is built in with frequency swapping function, which makes it easy for the power supply designers to optimize EMI performance and system cost.

On/Off Control

Pulling COMP pin below V_{ZDC} will immediately disable the gate output of LD5762P. Remove the pull-low signal to reset it.

Over Power Protection (OPP) - Latch Mode

The LD5762P features latch mode of smart OPP protection. Fig. 13 shows the waveform under fault condition. The feedback system will force the voltage loop toward the saturation and thus pull the voltage high across COMP pin (VCOMP). When the VCOMP ramps up to the OPP threshold of 4.6V and stays for longer than OPP delay time, the protection will be activated and then latch off the gate output to stop switching of the power circuit. The delay time is to prevent the false-triggering during power-on, turn-off transient and in peak load condition. As soon as the over load condition is removed, the controller will remain latched until the VCC drops lower than 6V. It is necessary to restart AC power-on recycling to resume the output.

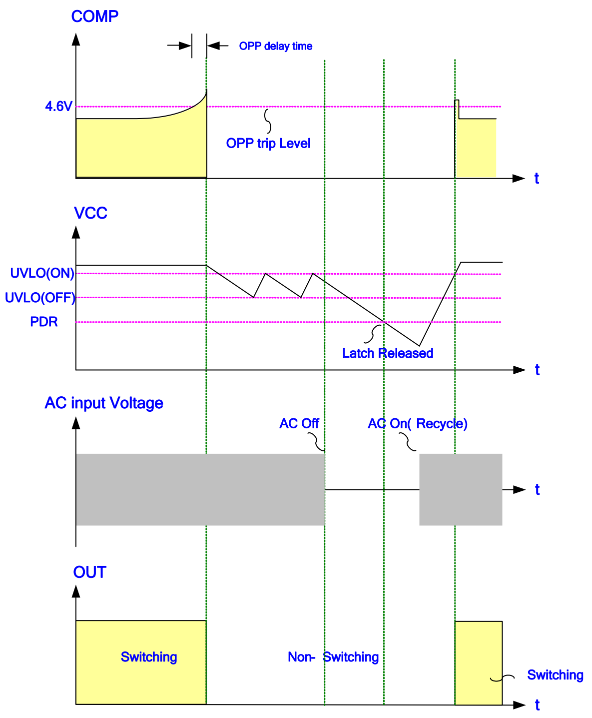


Fig. 13

Over Current Protection (OCP) –Latch Mode

When the switching current is higher than the OCP threshold, the internal counter counts up. When the total accumulated counting time is more than 1.7s, the controller triggers the OCP. This protection is latch mode function.

Over Voltage Protection on VCC (OVP) – Latch Mode

The V_{GS} ratings of the nowadays power MOSFETs are mostly with 32V maximum. To protect the V_{GS} from the fault condition, LD5762P is implemented with OVP function on VCC. As the VCC voltage is larger than the OVP threshold voltage, the output gate drive circuit will be shut off simultaneously and stop switching the power MOSFET.

The VCC OVP is latch-off type of protection. Once the VCC trips OVP level (which is usually caused by the feedback loop opened), it will be latched off and try to recover. Turn off AC power to let VCC fall below PDR level to release overvoltage protection. Then, restart the power to resume the operation. The de-latch level is defined by internal PDR. See Fig. 14 for its operation.

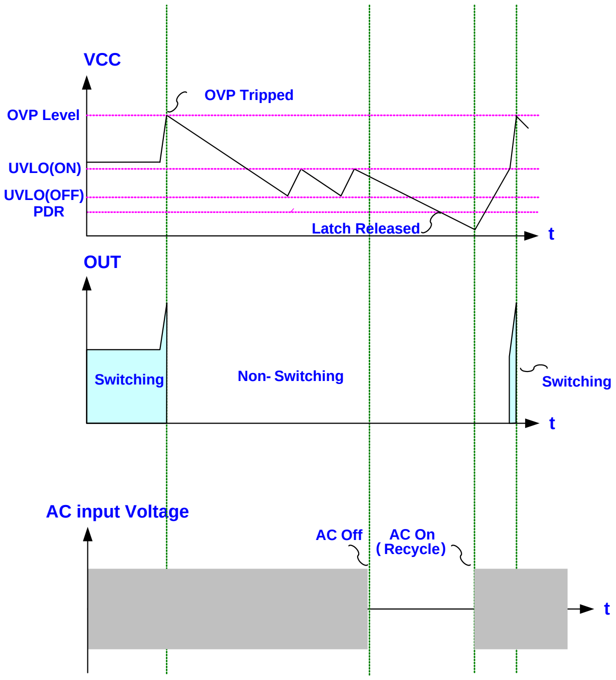


Fig. 14

On-Chip OTP – Auto Recovery

An internal OTP circuit is embedded inside the LD5762P to provide the worst-case protection for this controller. When the chip temperature rises higher than the trip OTP level, the output will be disabled until the chip is cooled down below the hysteresis window.

Under Voltage Protection on FB (FB_UVP) - Skip 1 Cycle

In order to prevent output short situation, LD5762P is implemented by FB_UVP. When the output load is shorted to ground, the voltage suddenly decreases to zero, which always reflects to auxiliary winding during the gate off region. Therefore, as VFB is lower than 0.5V during gate off region, and then the FB_UVP is triggered.

Over Voltage Protection on FB Pin (FB_OVP) – Latch Mode

An output overvoltage protection is implemented in the LD5762P. The auxiliary winding voltage can be reflected from secondary winding, in which the FB pin voltage is proportional to output voltage during the gate off time. OVP is worked by sensing the auxiliary voltage via the divided resistors R2, referring to Fig. 15. The equation of FB OVP is shown as follows.

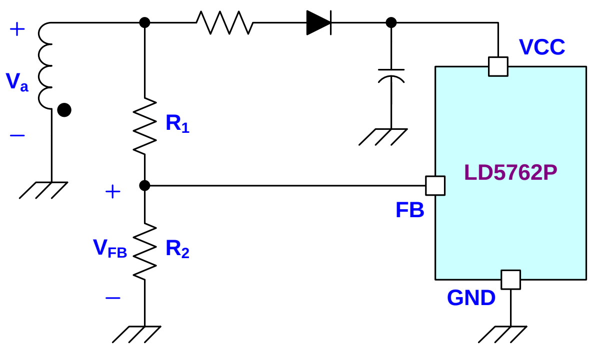


Fig. 15

$$R_2 = \frac{R_1 \times V_{FB\_OVP}}{V_a - V_{FB\_OVP}}$$

$$V_a = \frac{N_a}{N_S}(V_O + V_F)$$

V_{FB_OVP} is the FB pin OVP trip voltage level. V_a is the auxiliary winding voltage which reflects from the forward voltage V_F of schottky diode and output voltage V_O. N_S is turns ration of secondary-side winding.

If V_{FB} overs the FB_OVP trip level, the internal counter starts counting 8 cycles, and then LD5762P goes to latch mode.

Over Temperature Protection on CS Pin (CS OTP) - Latch Mode

LD5762P is implemented over temperature protection on CS pin which senses voltage to determine NTC status during gate off region. As V_{CS} is greater than 0.45V (VFB>1.5V) and continues for 35ms, CS_OTP is triggered, than LD5762P is in latch mode.

Pull-Low Resistor on the Gate Pin of MOSFET

The LD5762P consists of an anti-floating resistor at OUT pin to protect the output from damage in abnormally operation or condition due to false triggering of MOSFET. Even so, we still recommend adding an external one at the MOSFET gate terminal to provide more protection in case of disconnection of gate resistor R_G during power-on.

In such single-fault condition, as shown in Fig. 16, the resistor R_{GS} can provide a discharge path to avoid the MOSFET from being false-triggered by the current through the gate-to-drain capacitor C_{GD}. Therefore, the MOSFET should be always pulled low and placed in the off-state as the gate resistor is disconnected or opened in any case.

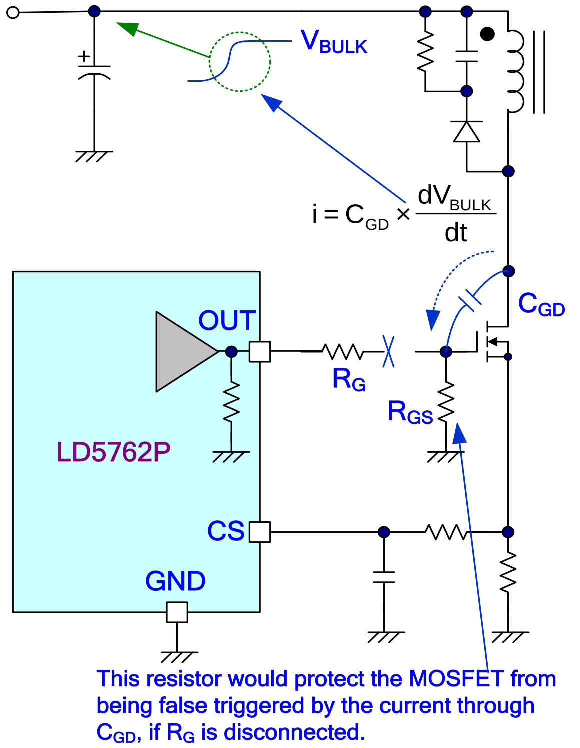


Fig. 16

Protection Resistor on the Hi-V Path

In some other Hi-V process and design, there may be a parasitic SCR caused around HV pin, VCC and GND. As shown in Fig. 17, a small negative spike on the HV pin may trigger this parasitic SCR and cause latch-up between VCC and GND. It may damage the chip because of the equivalent short-circuit induced by such latch-up behavior.

Hi-V technology will eliminate parasitic SCR in LD5762P. Fig. 18 shows the equivalent Hi-V structure circuit of LD5762P. So that LD5762P is more capable to sustain negative voltage than similar products. However, a 40KΩ resistor is recommended to be added in the Hi-V path to play as a current limit resistor whenever a negative voltage is applied.

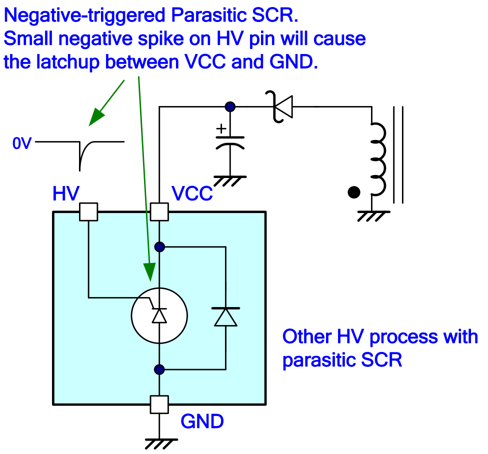

Negative-triggered Parasitic SCR.
Small negative spike on HV pin will cause
the latchup between VCC and GND.
0V
HV
VCC
Other HV process with
parasitic SCR
GND

Fig. 17

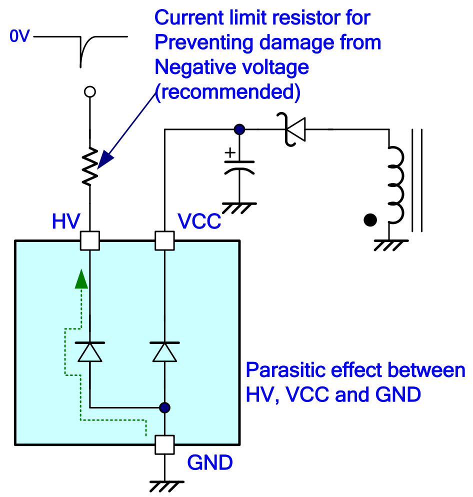
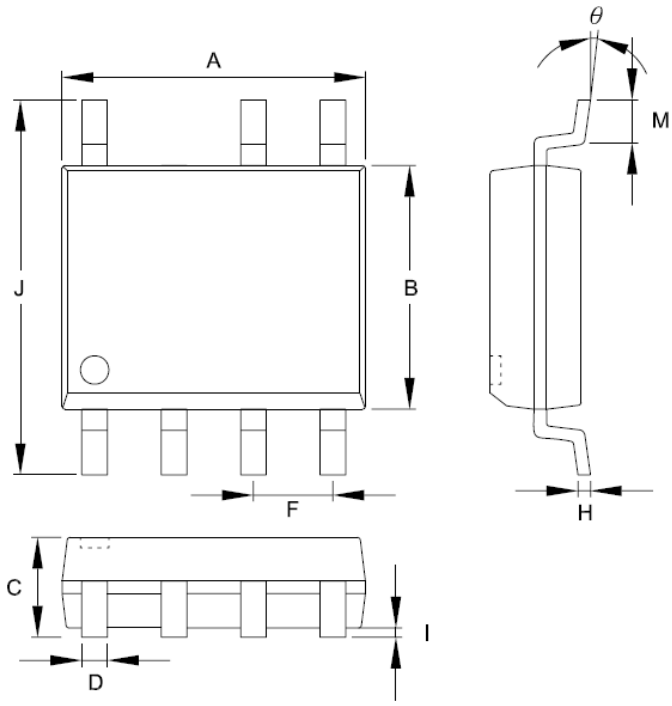

0V
Current limit resistor for
Preventing damage from
Negative voltage
(recommended)
HV
VCC
Parasitic effect between
HV, VCC and GND
GND

Fig. 18

Package Information

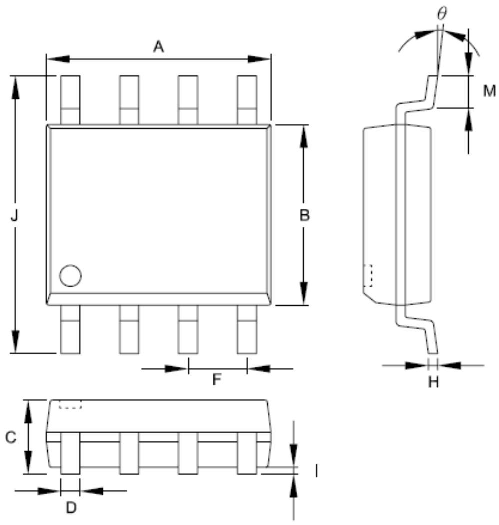
SOP-7



Symbols	Dimensions in Millimeters		Dimensions in Inch	
	MIN	MAX	MIN	MAX
A	4.801	5.004	0.189	0.197
B	3.810	3.988	0.150	0.157
C	1.346	1.753	0.053	0.069
D	0.330	0.508	0.013	0.020
F	1.194	1.346	0.047	0.053
H	0.178	0.254	0.007	0.010
I	0.102	0.254	0.004	0.010
J	5.791	6.198	0.228	0.244
M	0.406	1.270	0.016	0.050
θ	0°	8°	0°	8°

Package Information

SOP-8



Symbols	Dimensions in Millimeters		Dimensions in Inch	
	MIN	MAX	MIN	MAX
A	4.801	5.004	0.189	0.197
B	3.810	3.988	0.150	0.157
C	1.346	1.753	0.053	0.069
D	0.330	0.508	0.013	0.020
F	1.194	1.346	0.047	0.053
H	0.178	0.254	0.007	0.010
I	0.102	0.254	0.004	0.010
J	5.791	6.198	0.228	0.244
M	0.406	1.270	0.016	0.050
θ	0°	8°	0°	8°

Important Notice

Revision History

REV.	Date	Change Notice
00	05/02/2017	Original Specification